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PHASE I FINAL DEVELOPMENT REPORT FOR HIGH-RELIABILITY, LOW-COST--ETC(U)
FEB 77 N00039-76-C-0240
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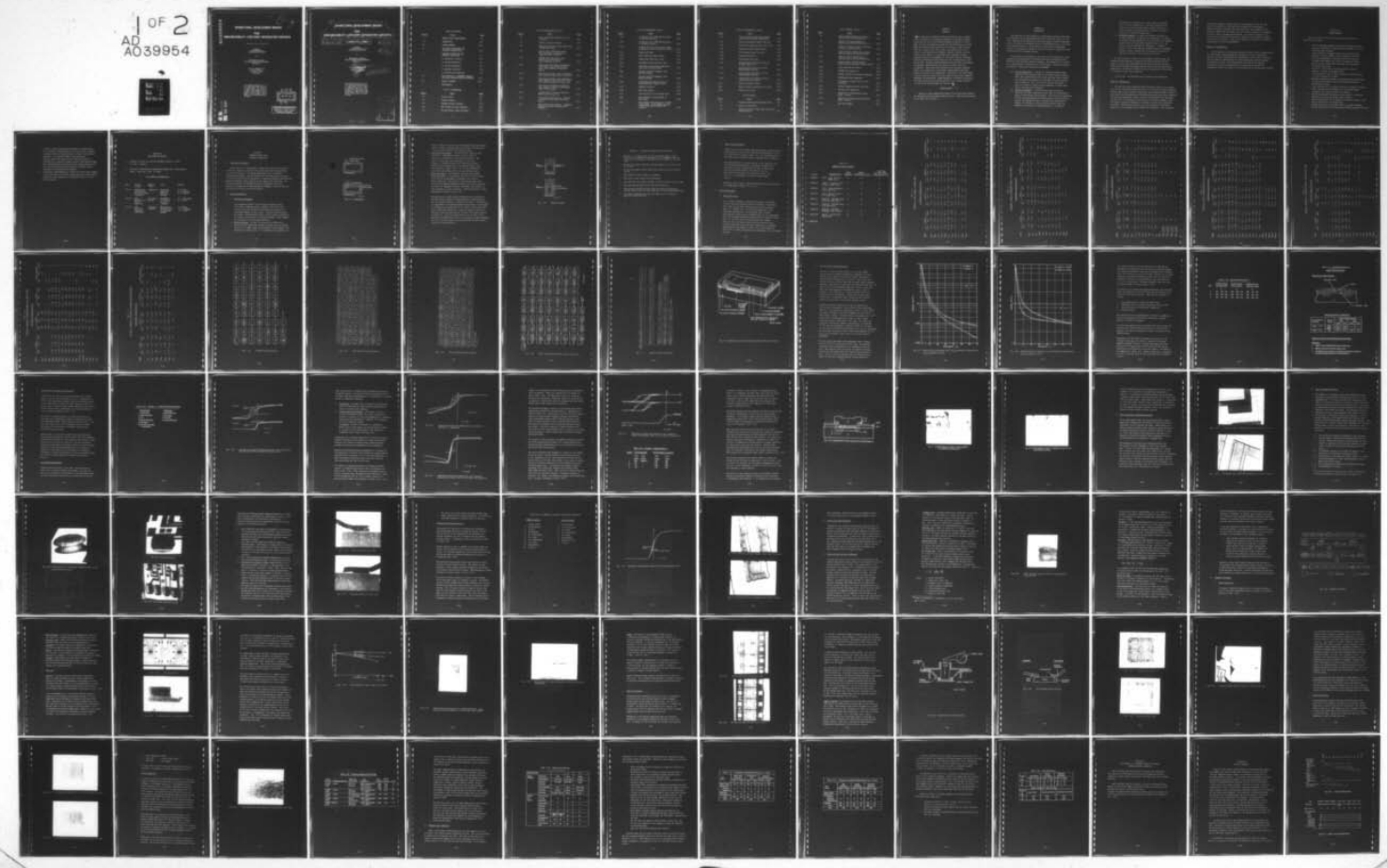

PHASE I FINAL DEVELOPMENT REPORT

FOR

HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS

3 FEBRUARY 1976 TO 3 FEBRUARY 1977

Prepared By
RCA Solid State Divison
Route 202, Somerville, N.J. 08876

For

DEPARTMENT OF THE NAVY
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.

Contract No. N00039-76-C-0240
Project No. 62762N
Subproject No. XF54586
Task No. 002

(6)

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SECTION I

ABSTRACT

The objective of Phase 1 of this investigation was to develop process feasibility, processing techniques, and automated assembly technology for dual-in-line plastic-packaged integrated circuits. Eight IC's were processed with trimetal interconnections, gold bond bumps and silicon nitride dielectric overcoating. These included three TTL circuits (5420, 5472, 5470), one Schottky TTL circuit (54S20), three CMOS circuits (CD4012B, CD4014A, CD4027A), and one linear circuit (CA741). A universal wafer processing sequence compatible with the requirements of each device type was developed. Electrical parameter specifications were met successfully for each device type. Critical wafer-processing steps have been investigated to determine reproducibility and effects on yield, cost, and reliability. Beam tapes were fabricated from polyimide supported copper and conditions for reproducibly high-strength inner-lead bonds to the device were established. Similarly, outer-lead bonding to plated steel or copper alloy lead frames on high speed automated equipment was facilitated. High-temperature accelerated reliability tests were initiated and problems related to the package materials of construction were analyzed and resolved.

ACKNOWLEDGMENT

Support for this program was provided to RCA Solid State Division by sponsorship from the Navelex Code 304 Group. Direction was provided by the NOSC Code 743 Group.

SECTION II
INTRODUCTION

The objective of this program is to investigate alternate approaches to MIL-M-38510 for achieving high-reliability integrated circuits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve a reliability level of 0.005%/1000 hours at 125°C with a 60% confidence level, a level that will meet military requirements without a cost penalty in excess of 20% over the cost of commercial, high-reliability plastic-packaged devices.

The approach to achievement of the goals of this program will be the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. The program will be carried out in three phases. During Phase I of the program - Sealed-Chip Process Utilization - three major tasks were accomplished:

(a) Process feasibility - in which the required photomasks were generated using existing masks to the maximum extent possible. Then, small quantities of each device type were made to assure that the masks and processes are available for the production runs of Phase II. Also, each device type was made using a matrix of carefully varied process parameters to assess their impact on yields and reliability.

(b) Process development - in which the processes required to fabricate the eight integrated-circuit types to be produced in Phase II were defined and documented. Silicon nitride passivation and the titanium-platinum-gold metallization system were used to achieve chip hermeticity and a corrosion-free metallization system. In addition, a silicon nitride overcoat layer was applied for protection of the metallization. A series of

experiments were carried out at each critical processing step to assure repeatability. Real-time indicators and accelerated life tests were used to assess the effects of process changes on reliability and to measure progress in achieving the required failure rate.

(c) Automated assembly - in which the assembly technology to be used in Phase II was defined and documented. The effect of assembly process parameters on cost and yield was assessed. Bonding tapes and lead-frames compatible with each of the device types were designed and fabricated. A number of devices of each type were then assembled using the automated assembly system. Reliability was continually monitored by real-time indicators and accelerated life tests.

At the conclusion of Phase I, the photomasks, wafer process, and assembly process required to fabricate the eight integrated-circuit types in the low-cost high-reliability device-fabrication phase were defined and documented and sample devices of each type were fabricated. Additionally, preliminary reliability data were generated to demonstrate the soundness of the chosen approach.

At this time, the production runs of Phase II were undertaken.

Phase II - Fabrication

The low-cost high-reliability device fabrication phase of the program will involve significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits will be constructed in both plastic and ceramic packages. This will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes will be defined and documented. The utilization

of existing equipment and mask sets will be demonstrated, and the cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions at wafer probe and final test will be used to monitor the production run and to assure process reproducibility. All devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and assembled.

Phase III - Reliability

The reliability of the devices produced in Phase II will be demonstrated. The conventional aluminum-metallized integrated circuits, packaged and tested to military high-reliability requirements, will be used as the baseline from which to appraise the new process developed under the program. In addition, the level of testing required over and above commercial screening to assure a reliable product for military end use will be determined, and the cost impact of this testing will be analyzed and verified.

SECTION III
ACCOMPLISHMENTS

Conclusions derived from the work during this period may be summarized as follows:

- The trimetallized versions of the eight integrated circuits resulted in electrical characteristics equivalent to circuits metallized with aluminum.
- A gate dielectric composed of 900 Å SiO_2 and 200 Å Si_3N_4 resulted in stable COS/MOS trimetal integrated circuits.
- Etch-rate measurements, radioactive sodium testing, and thickness measurements have shown that deposited silicon nitride junction passivating layers met the requirements for device fabrication.
- The 500 Å - 700 Å layer of platinum used for silicide formation resulted in optimized yield.
- A platinum layer, 1500 Å thick, provided an adequate barrier to Ti-Au diffusion up to 400°C.
- Magnetron sputtering provided a technique for the fabrication of trimetal MOS devices using the titanium-platinum-gold metallization system.
- A gold thickness of 1.5 microns resulted in optimized protective layer coverage, wafer throughput, and cost effectiveness consistent with reliable oxide step coverage.
- Dry-film photoresist techniques can be utilized to fabricate elevated bond pads with uniform cross sections.
- Device bond pads 1.0 mil in height are optimum in terms of cost, ease of fabrication, and reliability.
- Sputter etching of the platinum layer is a viable technique for the fabrication of gold metallized COS/MOS integrated circuits.

- A silicon nitride overcoating deposited in a plasma reactor to a thickness of approximately 12,000 Å provided an adherent conformal barrier to moisture-induced surface electroplating phenomena in the device trimetal interconnections.
- Unplated copper beam tapes and gold bond pads provided a metallurgical system that yielded uniform, high-strength bonds.
- The titanium-platinum gold metallization system eliminated the low bond pull-strength problem observed on COS/MOS devices fabricated with titanium-palladium-gold.
- Accelerated, high-temperature (200°C) life tests caused changes in the electrical and chemical characteristics of epoxy molding compounds; these changes had a catastrophic effect on device characteristics.

SECTION IV

RCA PATENT DISCLOSURES

1. Trimetal Structure for Auto Dip Assembly, Docket No. 70950. W. Lewis, S. Ahrens.

2. Combination Glass/Nitride Passivating Overcoat for a Semiconductor Device. Docket No. 71148. W. Lewis.

RCA TECHNICAL PRESENTATIONS

Date	Society Sponsor	Meeting Place	Title	Authors
3/1/77	NEPCON, West International Microelectronics Conference	Anaheim, CA	Structural Aspects of Beam-Tape Bonding	A. S. Rose F. E. Scheline T. V. Sikina
4/14/77	IEEE Reliability of Physics Symposium	Las Vegas, Nevada	Reliability of Trimetal Plastic IC Packages	H. J. Khajezadeh A. S. Rose
5/17/77	IEEE Electronic Components Conference	Arlington, Virginia	Metallurgical Considerations for Beam-Tape Assembly	A. S. Rose F. E. Scheline T. V. Sikina

SECTION V

DETAILED FACTUAL DATA

TECHNICAL DISCUSSION

A. Objectives of Phase I

During Phase I of this program to design and develop low-cost high-reliability integrated circuits, three major tasks have been performed, (1) Process Feasibility (2) Process Development, and (3) Assembly Technology Development. Process Feasibility has demonstrated the extent to which the silicon-nitride passivated, titanium-platinum-gold metallization system is compatible with existing circuit designs and photomasks. The Process Development and Assembly Technology Development tasks have defined and documented the wafer-process and assembly techniques required to achieve the desired level of reliability.

B. Process Feasibility

1. Photomask Development

The photomasks required for the eight integrated circuit types (CA741, CD4012B, CD4014A, CD4027B, 5420, 54S20, 5470 and 5472) have been designed, fabricated and proven out by processing samples of each circuit. Some minor modifications were made to existing mask layouts to either enhance reliability or optimize the structure for automated bonding. These changes are delineated in the following sections:

a. Contact Coverage. In order to enhance the reliability of silicon nitride passivated titanium, platinum, gold metallized circuits, the design rules for metallization were changed. This modification, shown in Fig. V-1, eliminates the possibility of

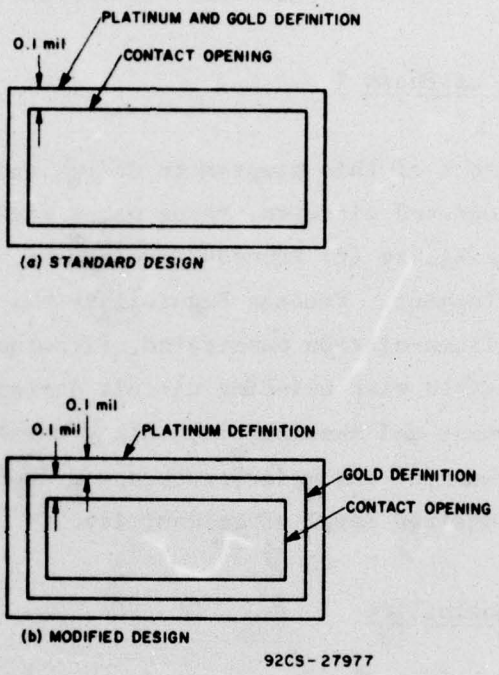


Fig. V–1 – Contact areas.

contact between the silicon and the deposited gold and titanium layers in contact openings, which could lead to the formation of a low melting point (∿280°C) eutectic alloy.

b. Protective Layer Design. A silicon nitride overcoat layer deposited at temperatures between 250°C and 300°C is required for protection of the gold metallization. This layer is etched open over bond bumps to facilitate bonding. To prevent attack of the underlying junction sealing silicon nitride layer, the standard design rules were modified as shown in Fig. V-2 to assure termination of the bond pad opening etch on the gold metallization.

c. Bond Pad Location. To facilitate automated gang bonding using beam tapes, it is essential that the bond pad locations on the device be specified in accordance with rational design guidelines. The principal requirements among these rules involve minimum separation between bond bumps, peripheral straight line alignment along the chip edges, and avoidance of bump placement at corner locations. A detailed outline of these requirements is given in Table V-1.

The observation of these rules in bond-pad layout provides for uniform pressure during the thermocompression bonding sequence when the bonding thermode is aligned to the bumps. Additionally, the requirement for a minimum spacing between bumps is established to accomodate the capabilities of the chemical milling processes used in beam-tape fabrication. Beam-tape fingers, 0.0014-inch thick and 0.003-inch wide require a minimal intradigital spacing of 0.003 inch. With the single exception of the CA741, which required a revised bond-pad layout to accomodate automated assembly, all of the wire-bond pads on the remaining devices were suitably located for bump fabrication.

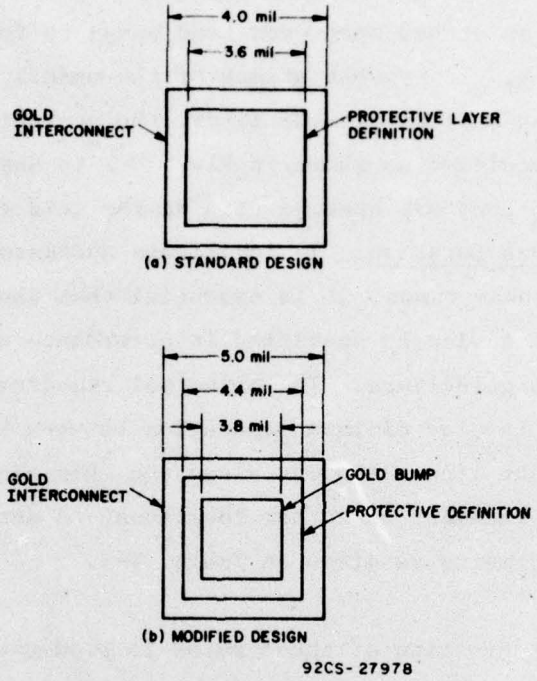


Fig. V-2 Bond-pad design.

TABLE V-1 - Automated Assembly Device Design Rules

- Maintain a 1:1 aspect ratio at the chip layout stage. If the chip must be rectangular in geometry, it is recommended that the longer side be expanded in the Y-direction (cross-web on the beam tape).
- Maintain pad layout uniformity and bump symmetry on all four sides of the chip.
- The nominal design centers listed below should be used as minimum values.
- Bond pads must form a square or rectangle.
- Bond pads at chip corners are unacceptable.
- Bond pads must be located a minimum of 0.004 inch from the chip edge.
- Bond pads spacing shall be not less than 0.003 inch.
- The separation between the bond pads and adjacent interconnect pattern shall be not less than 0.002 inch to avoid possible shorting.
- The nominal dimensions for the gold bumps shall be 0.004-inch square by 0.001-inch thick.

2. Sample Characterization

Samples of seven of the eight integrated-circuit types fabricated during Phase I of the contract have been characterized at -55°C, 25°C, and +125°C as shown in Table V-2. The characterization of the eighth type, the CA741, will be completed early in Phase II.

Although the CA741 is a popular device in the commercial area, the MIL-M-38510 specification is extremely stringent for aluminum as well as trimetallized circuits. With several minor process modifications, the CA741 has met the MIL-M-38510 specification with acceptable yield. Two wafer lots are currently in process to verify these results.

Parametric data on each of the seven devices ready for production are summarized in Tables V-3 to V-9.

C. Process Development

1. Wafer Fabrication

The processes required to fabricate the bipolar and COS/MOS circuits under the contract have been developed. Generalized flow charts of the wafer fabrication processes are shown in Figs. V-3 through V-7. Of particular importance is the successful elimination of the previously used titanium-palladium-gold system used on COS/MOS wafers and its replacement with the titanium-platinum-gold system used for bipolar circuits. Fig. V-8 shows the silicon nitride passivated trimetal structure with a silicon nitride protective overcoat layer. Critical processing areas have been investigated to determine reproducibility and effects on yield, cost, and reliability. The results of these investigations are delineated in the following sections.

TABLE V-2

DEVICE STATUS REVIEW

	TA No.	DESCRIPTION	TEST PROGRAM	SAMPLE CHARACTERIZATION	100-UNIT HI-LOW TEMP. CHARACTERIZATION
1.	TA10151	5420 Dual 4-Input NAND Gate	C	C	C
2.	TA10152	54S20 Schottky Dual 4-Input NAND Gate	C	C	C
3.	TA10153	5470 Edge-Triggered J-K Flip Flop	C	C	C
4.	TA10154	5472 Master Slave J-K Flip Flop	C	C	C
5.	TA10155	CD4012B COS/MOS Dual 4-Input NAND Gate	C	C	C
6.	TA10156	CD4027B COS/MOS Dual J-K Flip-Flop	C	C	C
7.	TA10219	CD4014A COS/MOS 8-Stage Shift Register	C	C	C
8.	TA10158	CA741 Operational Amplifier	C	C	C

C = COMPLETE

TABLE V-3

TA10151 5420 DUAL 4 INPUT GATE

ELECTRICAL CHARACTERISTICS

TEST	-55°C			25°C			+125°C			Spec.Limits		
	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Max.	Units
V_{OL}	.213	.232	.258	.245	.260	.284	.320	.342	.354	-	0.4	V
V_{OH}	2.06	2.70	2.82	2.29	2.79	3.15	2.26	2.79	2.85	2.4	-	V
I_{OS}	-35.2	-33.4	-22.4	-35.2	-33.2	-22.7	-29.5	-28.6	-19.3	-55	-20	mA
I_{IH1}	5.0	8.3	22.2	10.8	16.2	30.4	8.8	26.8	46.4	-	40	µA
I_{IH2}	8.0	12.6	105.2	16.8	25.7	71.2	11.2	49.8	73.6	-	100	µA
I_{IL}	-1.056	-1.122	-1.224	-1.144	-1.175	-1.288	-.927	-1.069	-1.176	-1.6	-.7	mA
I_{CCL}	7.08	7.28	7.88	7.44	7.6	8.24	6.84	7.00	7.28	-	10.0	mA
I_{CCH}	2.32	2.41	2.57	2.41	2.48	2.61	2.21	2.27	2.38	-	3.3	mA
V_{IC}	-	-	-	-.912	-1.002	-1.292	-	-	-	-1.5	-	V
T_{PHL}	6.4	7.6	9.1	5.0	5.6	6.5	4.9	5.2	5.7	3	24	NS
T_{PLH}	7.3	9.3	10.9	8.9	12.4	17.4	12.5	20.0	27.6	3	27	NS

TABLE V-4

TA10152 54S20 SCHOTTKY DUAL 4 INPUT GATE

ELECTRICAL CHARACTERISTICS

TEST	-55°C			25°C			+125°C			Spec.Limits		
	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Max.	Units
V_{OH}	2.67	2.69	2.73	2.94	2.95	2.96	3.02	3.10	3.18	2.5		V
V_{OL}	0.40	0.46	0.46	0.36	0.39	0.41	0.33	0.37	0.40	0.2	0.5	V
V_{IC}				-0.69	-0.71	-0.72				-1.2		V
I_{CEX}	≈0	≈0	12	≈0	1	34	50	63	112		250	µA
I_{IH1}	≈0	0.1	8.6	0.2	0.6	19	5.6	8	53		50	µA
I_{IH2}	≈0	0.4	38	0.3	1.0	77	8.8	12.7	98.4		1000	µA
I_{IL}	-1.8	-1.7	-1.6	-1.9	-1.8	-1.7	-1.7	-1.6	-1.5	-2	-1	mA
I_{OS}	-70	-67	-64	-75	-73	-72	-69	-68	-66	-100	-40	mA
I_{CCH}	6.0	6.1	6.2	6.5	6.4	6.3	5.9	5.8	5.7		8	mA
I_{CCL}	12.9	12.7	12.5	14.2	14.0	13.8	13.5	13.3	13.2		18	mA
T_{PHL}		7.2			6.7			6.8		2	9	NS
T_{PLH}		6.9			6.7			7.8		2	9	NS

TABLE V-5

TA10153 5470 EDGE-TRIGGERED J.K. FLIP FLOP

ELECTRICAL CHARACTERISTICS

TEST	-55°C			+25°C			+125°C			Spec.Limits		
	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Max.	Units
V_{OH}	2.71	2.73	3.59	3.04	3.06	3.76	3.41	3.43	3.46	2.4	-	V
V_{OL}	.001	.273 .002	.305	.001	.278 .002	.301	.001	.337 .002	.362	-	0.4	V
V_{IC}	-	-	-	-.89	-.96	-1.13	-	-	-	-1.5	-	V
I_{IL1}	-.871	-.920	-.959	-.881	-.972	-1.017	-.783	-.886	-.935	-1.6	-0.7	mA
I_{IH1}	5.6	12.0	22.6	11.5	22.7	38.0	18.2	33.8	59.2	-	40	µA
I_{IH2}	7.9	16.7	30.3	17.4	32.0	51.4	26.4	48.1	81.2	-	100	µA
I_{IH3}	14.5	18.2	25.5	28.2	35.0	45.2	44.4	48.8	64.4	-	80	µA
I_{IH4}	14.3	24.6	40.8	32.8	48.0	70.0	50.0	67.8	96.0	-	200	µA
I_{OS}	-21.7	-22.4	-25.7	-23.3	-23.7	-26.5	-20.3	-21.0	-23.7	-57	-20	mA
I_{CL}	10.8	14.2	17.7	13.5	14.0	17.0	12.4	12.9	16.0	-	30	mA
F_{MAX}		15			18			16		7.5		MHz
T_{PLH} (clear to output)		19			23			29		5	62	NS
T_{PHL} (clear to output)		20			15			17		5	62	NS
T_{PLH} (clock to output)		32			30			36		5	62	NS
T_{PHL} (clock to output)		29			23			24		5	62	NS

TABLE V-6

TA10154 5472 MASTER SLAVE J.K. FLIP FLOP

ELECTRICAL CHARACTERISTICS

TEST	-55°C			25°C			+125°C			Spec.Limits		
	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Max.	Units
V_{OH}	1.04	2.73	2.76	2.84	3.01	3.02	2.56	3.39	3.41	2.4	-	V
V_{OL}	.236	.257	.280	.248	.276	.298	.316	.349	.984	-	0.4	V
V_{IC}	-	-	-	-.79	-.93	-1.00	-.63	-.81	-.89	-1.5	-	V
I_{IL1}	-1.032	-1.120	-1.200	-1.056	-1.132	-1.196	-.940	-1.009	-1.076	-1.6	-0.7	mA
I_{IL2}	-1.91	-2.01	-2.13	-1.98	-2.8	-2.16	-1.83	-1.88	-1.97	-3.2	-1.4	mA
I_{IL3}	-1.036	-1.118	-2.048	-1.056	-1.116	-1.184	-.984	-1.016	-1.168	-1.6	-0.7	mA
I_{IH1}	.8	1.9	3.7	1.6	3.4	6.4	4.4	7.5	12.0	-	40	µA
I_{IH2}	0.0	0.1	0.3	0.0	0.1	0.1	0.0	0.1	0.1	-	100	µA
I_{IH3}	12.8	16.4	26.4	22.4	27.2	46.4	36.8	44.0	73.6	-	80	µA
I_{IH4}	8.4	16.8	39.2	16.0	28.0	78.4	30.4	45.6	153.6	-	200	µA
I_{IH5}	-321	-340	-358	-348	-376	-404	-312	-368	-392	-500	-50	µA
I_{OS}	-25.7	-27.1	-28.1	-25.5	-26.8	-27.8	-22.4	-22.8	-33.2	-57	-20	mA
I_{CC}	11.92	12.8	15.20	12.64	13.04	14.72	11.44	11.8	13.04	-	20	mA
FMAX				5	-	-				5	-	MHz
T_{PLH1}				12.5	14.0	15.2				5	25	NS
T_{PHL1}				20.9	22.3	23.4				5	40	NS
T_{PLH2}				14.6	16.4	17.8				5	30	NS
T_{PHL2}				23.0	24.5	25.9				5	40	NS

TABLE V-7

TA10155 CD4012B COS/MOS DUAL 4 INPUT NAND GATE

ELECTRICAL CHARACTERISTICS

TEST	-55°C			25°C			+125°C			Spec. Limits		
	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Max.	Units
V_{IC+}				.76	.77	.78					1.5	V
V_{IC-}				-.71	-.72	-.73				-6.0		V
I_{SS}				.0	-.6	-9	-350	-550	-1500	-750		NA
V_{OH1}	4.7	4.8	4.9	4.7	4.8	4.9	4.7	4.8	4.9	4.2		V
V_{OH2}	5.00	5.01	5.01	5.00	5.01	5.01	4.97	5.00	5.01	4.95		V
V_{OH3}	11.76	12.20	12.32	11.76	12.10	12.32	11.70	12.10	12.30	11.25		V
V_{OL1}	.051	.058	.077	.053	.060	.067	.056	.064	.128		0.7	V
V_{OL2}	.000	.001	.001	.000	.001	.002	.002	.004	.06		.05	V
V_{OL3}	.016	.072	.336	.064	.242	.608	.256	.624	1.024		1.25	V
I_{IH1}				.0	.4	8.9					8.0	NA
I_{IL1}				+.96	-.2	-.72				-8.0		NA
I_{IL2}				+.36	-.03	-.15	-7.8	-5.8	-4.2	-45		NA
T_{PHL}					70					15	290	NS
T_{PLH}					55					15	290	NS
T_{THL}					115					40	575	NS
T_{TLH}					102					35	610	NS

TABLE V-8

TA10156 CD4027A COS/MOS DUAL J.K. FLIP FLOP

ELECTRICAL CHARACTERISTICS

TEST	-55°C			+25°C			+125°C			Spec.Limits		
	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Max.	Units
V_{IC+}	-	-	-	.654	.738	.968	-	-	-	-	1.5	V
V_{IC-}	-	-	-	-.66	-.72	-0.8	-	-	-	-6.0	-	V
I_{SS}				.000	-.004	-1.304	.4	.04	-156	-2.5	-	µA
V_{OH1}	2.92	4.92	4.97	.61	4.90	4.91	4.78	4.89	4.99	4.5	-	V
V_{OH2}	1.24	5.02	5.04	.75	5.01	5.01	1.61	5.01	5.01	4.95	-	V
V_{OH3}	1.28	12.57	12.64	3.96	12.53	12.54	12.19	12.53	12.54	11.25	-	V
V_{OL1}	.128	.154	1.212	.144	.162	.236	.112	-153	.200	-	0.5	V
V_{OL2}	.000	.002	1.648	.000	.001	1.798	.000	.002	.525	-	.05	V
V_{OL3}	.002	.007	1.958	.001	.003	1.971	.000	.003	.259	-	1.25	V
V_{OL4}	.001	.004	1.907	.000	.002	1.676	.000	.002	.446	-	.05	V
V_{OH4}	1.06	5.02	5.04	.97	5.01	5.01	1.51	5.01	5.01	4.95	-	V
$V_{I(CL1)}$	.001	.002	.871	.001	.002	.172	.001	.002	.203	-	0.5	V
$V_{I(CL1)}$	.001	.002	.734	.001	.002	.121	.001	.002	.358	-	0.5	V
I_{IH1}	-	-	-	-.04	.04	1.24	-	-	-	-	10	NA
I_{IH2}	-	-	-	-.08	.01	.60	0	8.6	105	-	45	NA
I_{IL1}	-	-	-	-1.44	-.04	+.40	-	-	-	-10	-	NA
I_{IL2}				-.17	-.01	.14	-3.4	-1.3	-.5	-45	-	NA

TABLE V-9

TA10219 CD4014A COS/MOS 8 STAGE SHIFT REGISTER

ELECTRICAL CHARACTERISTICS

TEST	-55°C			+25°C			+125°C			Spec.Limits		
	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Ave.	Max.	Min.	Max.	Units
I_{IL}	.18	.083	-7.84	4.48	.35	-5.44	.08	-.698	-6.72	-10	-	NA
I_{IH}	-.52	-.36	9.94	-.32	1.41	20.32	-.2	20.0	25.6	-	10	NA
V_{OL1}	.184	.204	.340	.200	.214	.340	.196	.209	.316	-	0.5	V
V_{OL2}	0	1.0	369	0	1.0	25.0	2.0	3.0	145	-	10	mV
V_{OH1}	4.74	4.80	4.82	4.69	4.73	4.75	4.69	4.73	4.75	4.5	-	V
V_{OH2}	14.76	15.03	15.04	14.97	15.03	15.04	14.76	15.03	15.03	14.99	-	V
I_{SS}	≈0	≈0	-.07	≈0	-.04	-.1	-2	-4.7	-8.3		-5.0	uA

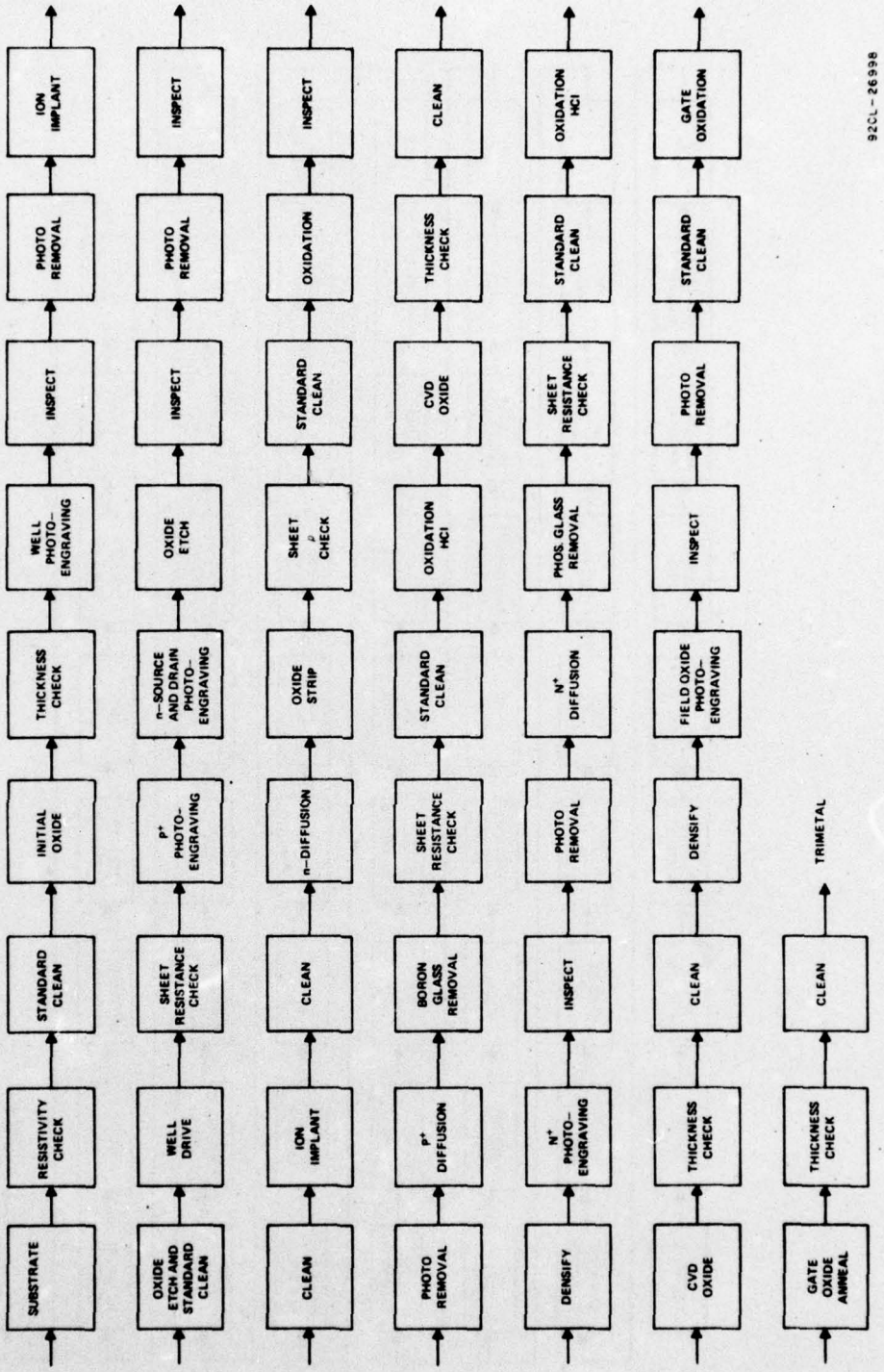


Fig. V-3 COS/MOS process flowchart.

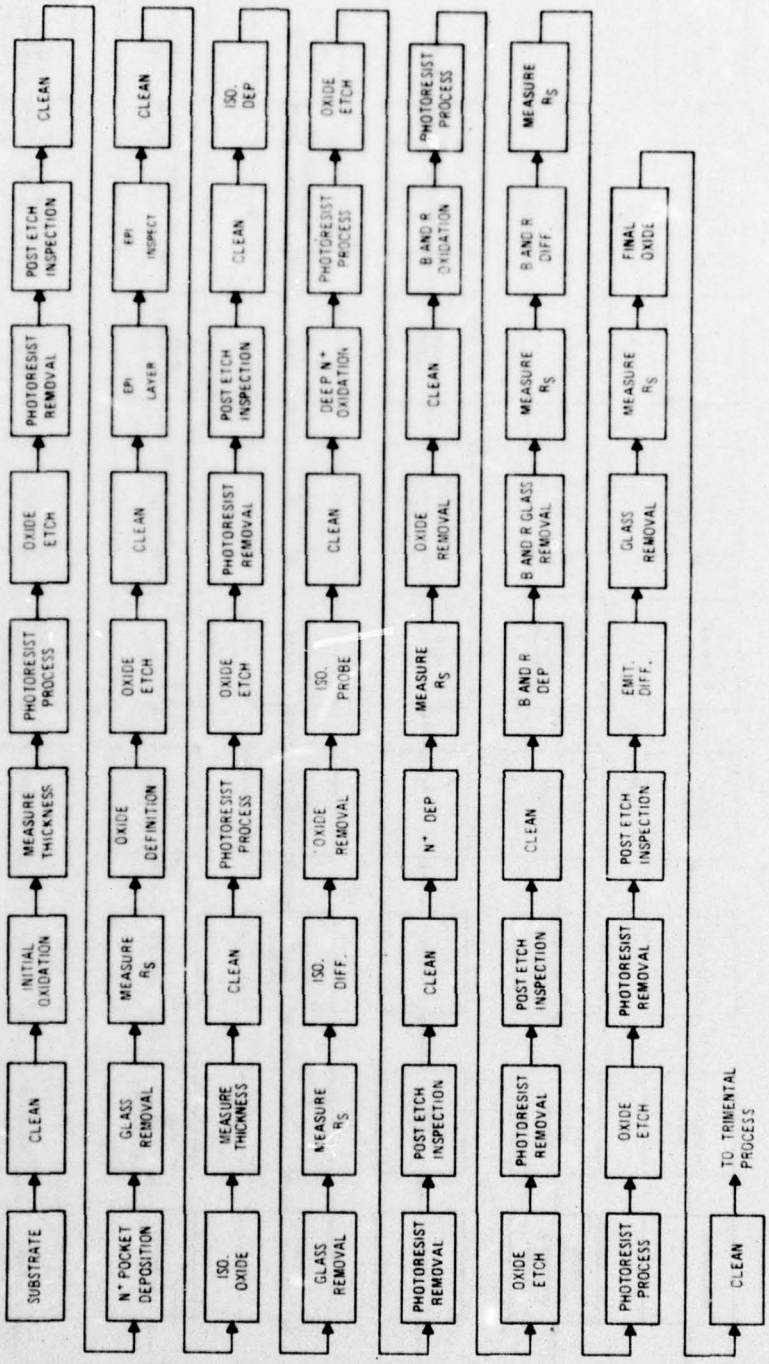


Fig. V-4 TTL Schottky process flowchart.

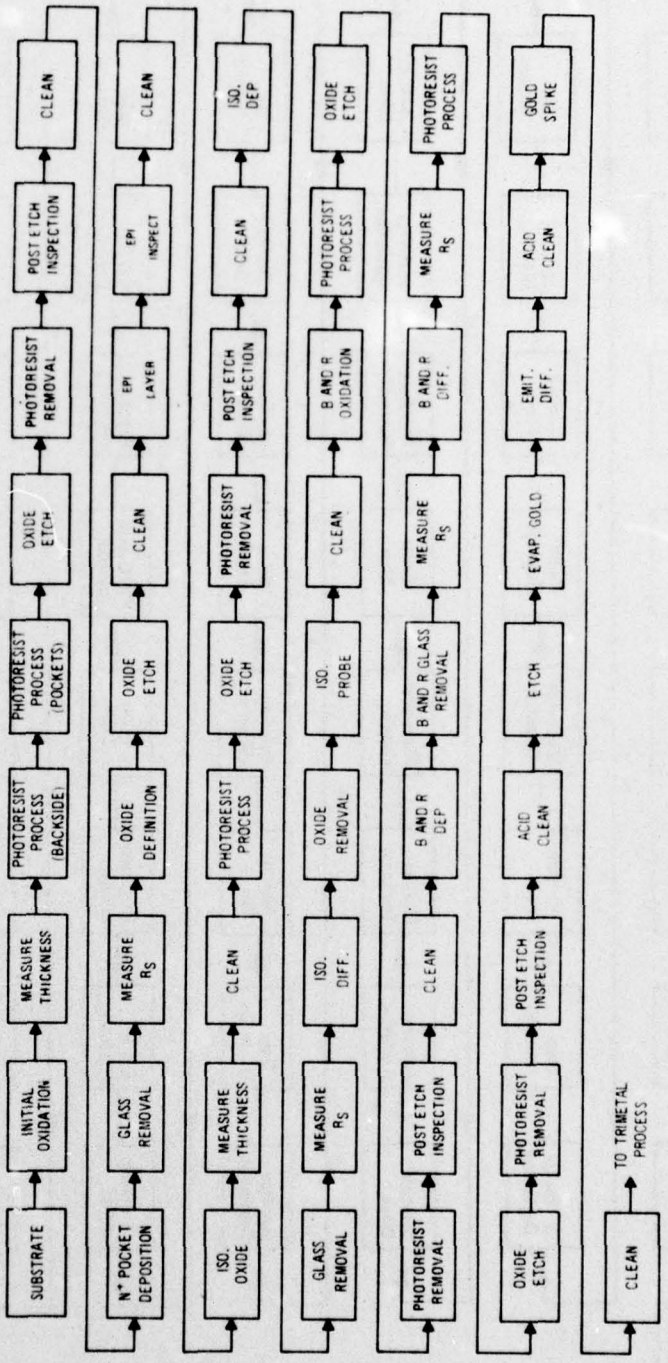


Fig. V-5 TTL gold-doped process flowchart.

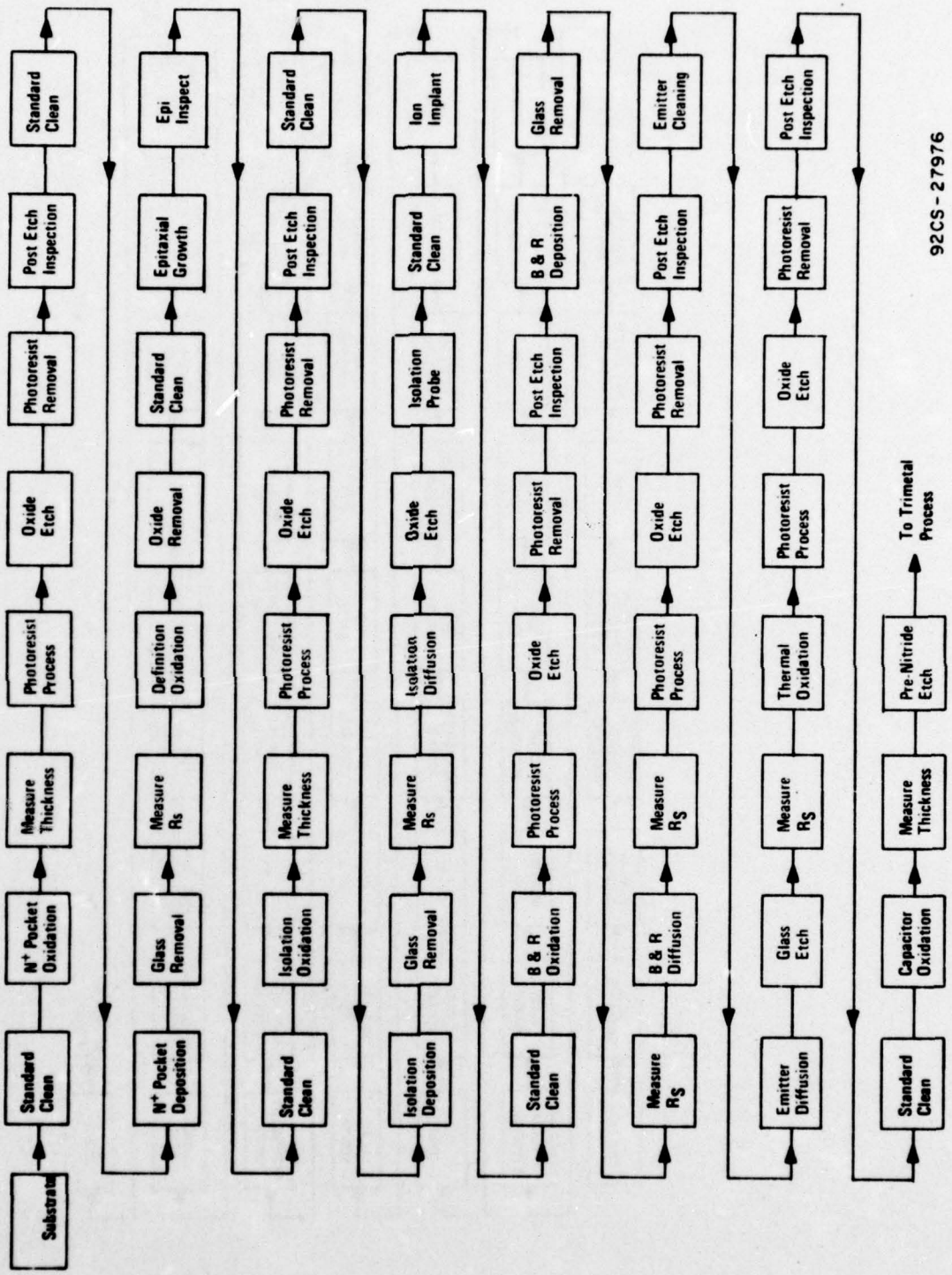


Fig. V-6 CA741 operational-amplifier process flow chart.

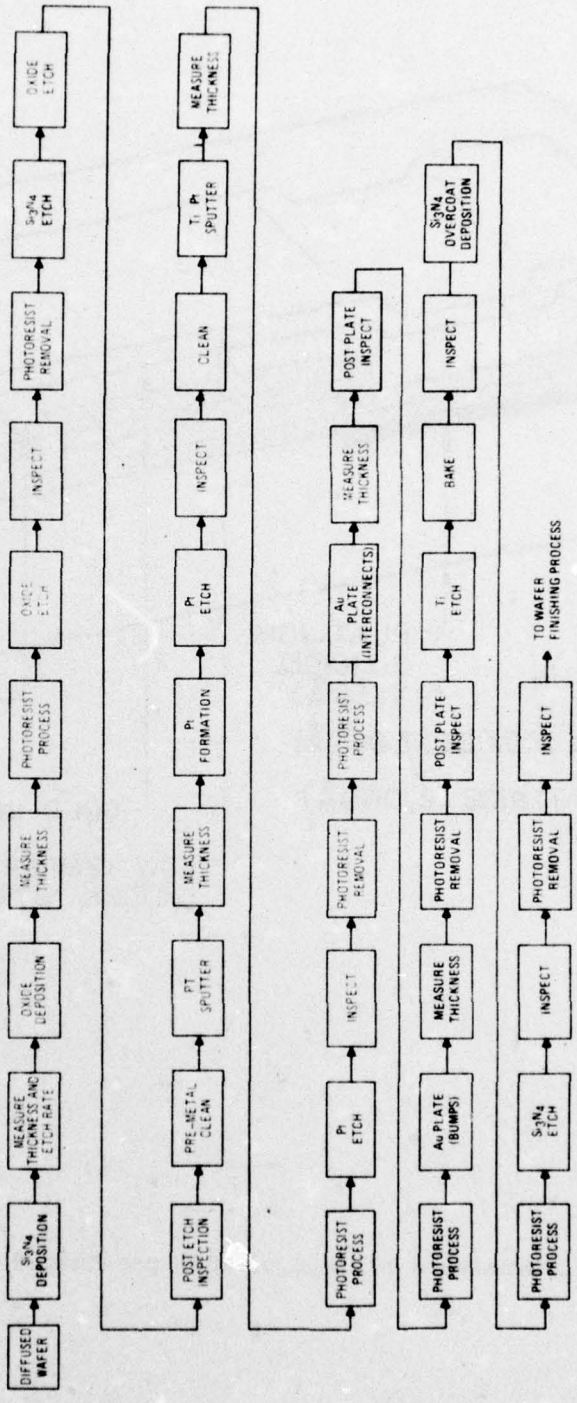


Fig. V-7 Trimetal process flow chart.

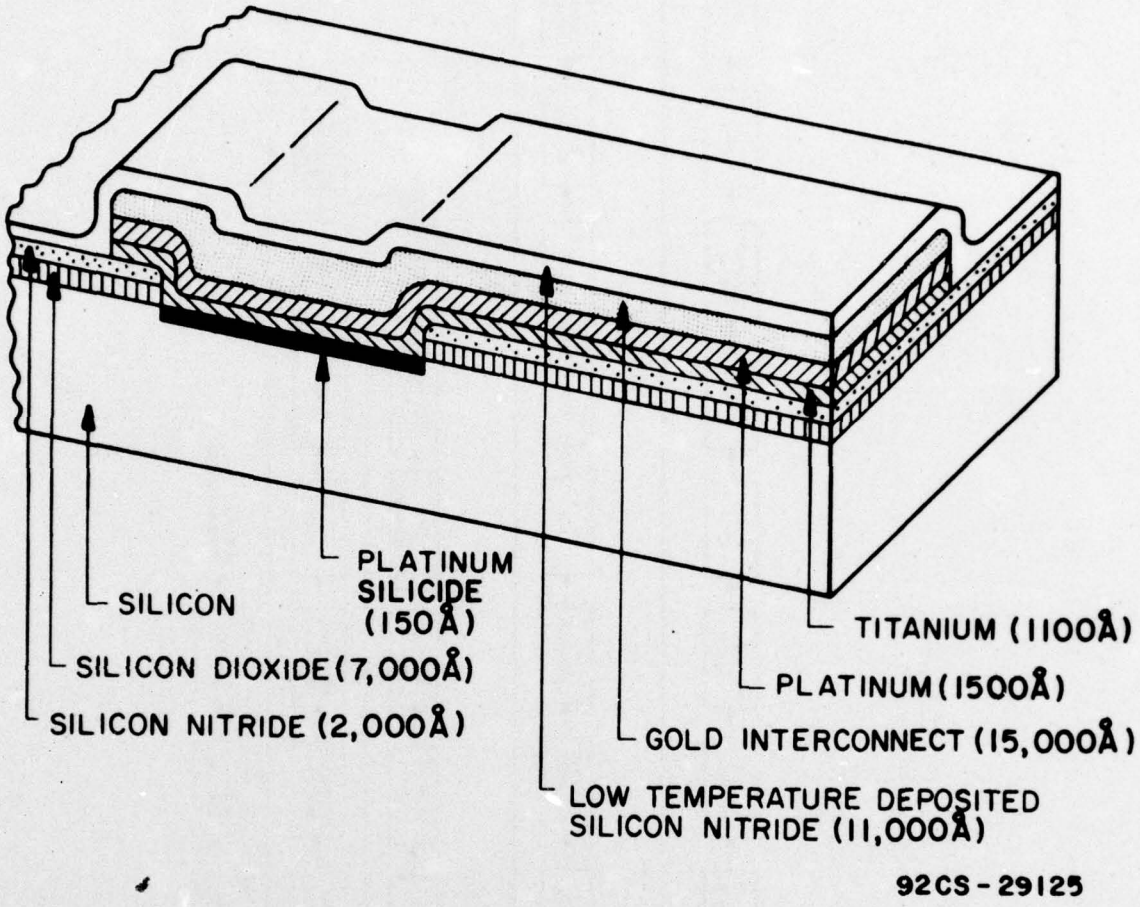


Fig. V-8 Dimensioned silicon nitride passivated trimetal structure.

2. Silicon Nitride Characterization

The use of silicon nitride (Si_3N_4) as a junction sealant derives from its superior qualities in comparison to silicon dioxide (SiO_2), particularly silicon dioxide deposited by a chemical-vapor deposition (CVD) process. Si_3N_4, which has a higher dielectric constant than SiO_2, provides higher breakdown voltages. When used as a thin film over thermally grown SiO_2, it acts as a seal for underlying pinholes in the SiO_2 layer that might otherwise cause metal-to-substrate shorts. Silicon nitride is very effective as a barrier against alkali ion penetration into the surface. Sodium ions, in particular, are the cause of excessive mobile charge and cause surface inversion layers and/or reverse-bias leakage currents.

Radioactive-tracer evaluations are used to determine the effectiveness of deposited silicon nitride films as alkaline barriers. Test wafers are coated with a layer of Si_3N_4, 2000 Å for bipolar circuits and 200 Å for COS/MOS circuits, over a 3000 Å layer of SiO_2. A 0.2-mil solution containing 1.31×10^{-6} atoms Na and 4 microcuries Na_{22} is used to coat a nickel electrode, which is dried under a heat lamp. The wafers are coated with this tracer element by evaporation at a pressure of 10^{-6} torr and subsequently annealed at 600°C for 22 hours. At this point, the surface radioactivity (R) of Na_{22} is determined. The test wafers are then etched to remove approximately 10 Å of Si_3N_4, and the surface radioactivity of the fresh surfaces determined.

The test wafers are etched three additional times to remove totals of 30 Å, 50 Å, and then 65 Å of Si_3N_4. The residual radioactivity as a precentage of R is determined after each etch. The results of this evaluation for samples of silicon nitride from the system used for IC fabrication are shown in Figs. V-9 and V-10, and indicate that the deposited Si_3N_4 layers are effective barriers against sodium penetration.

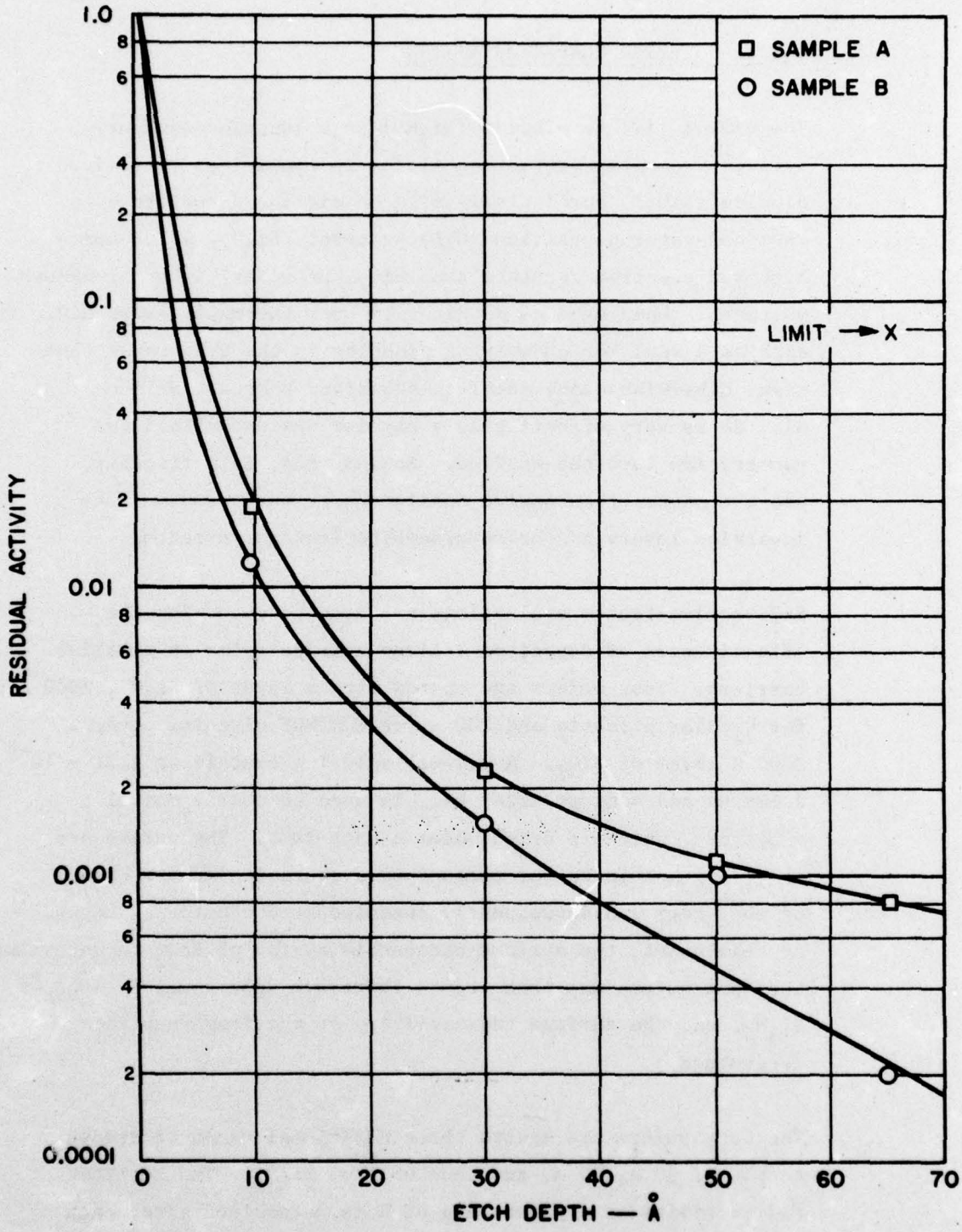


Fig. V-9 Bipolar Si_3N_4 passivating layer, Na_{22} penetration characteristic. Si_3N_4 thickness is 2000 Å.

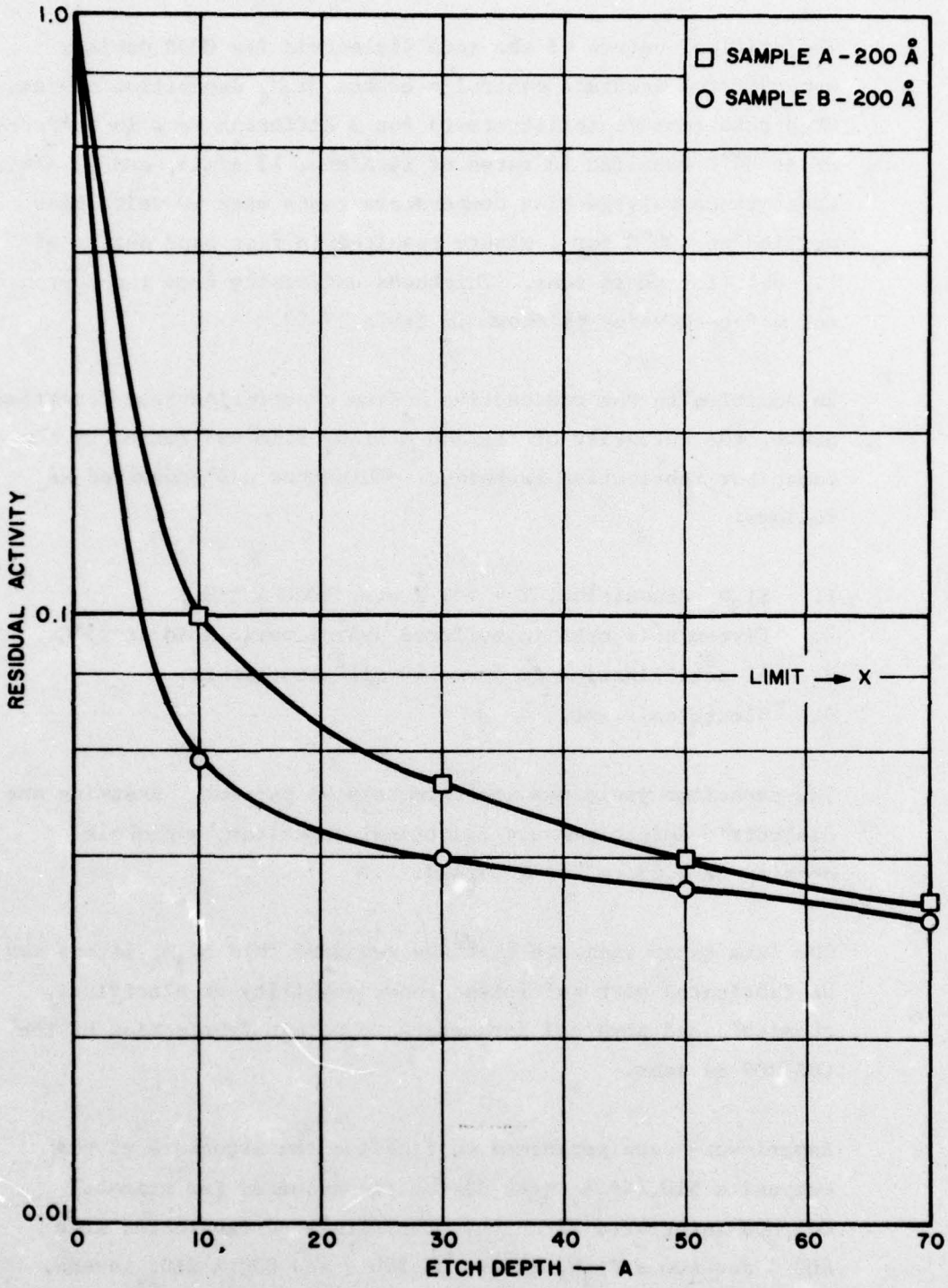


Fig. V-10 COS/MOS Si_3N_4 gate dielectric, Na_{22} penetration characteristic. Si_3N_4 thickness is 200 Å.

The critical nature of the gate dielectric for CMOS devices necessitates accurate control over the Si_3N_4 deposition system. Etch rate reproducibility tests for 3 different runs in buffered HF at 24°C resulted in rates of 14 Å/min, 15 Å/min, and 13 Å/min. Capacitance voltage-bias temperature tests with 10 volts bias applied at 300°C for 1 minute resulted in flat band shifts of 0.1 volt for these runs. Thickness uniformity from run-to-run and wafer-to-wafer is shown in Table V-10.

In addition to the radioactive sodium penetration test described above, the integrity of the 200 Å Si_3N_4 film was tested by the capacitor fabrication technique. This test was conducted as follows:

1. Si_3N_4 deposition, T = 200 Å over 3000 Å SiO_2.
2. Five-minute etch in buffered hydrofluoric acid at 25°C.
3. Al metallization to form 160 mil^2 capacitors.
4. Electrical test.

The capacitor yield was approximately 95 percent. Assuming one dielectric defect per non-functional capacitor, a pinhole density of 4.63/cm^2 is attained.

The data taken indicate that the required thin Si_3N_4 layers can be fabricated with sufficient reproducibility of electrical, chemical, and physical parameters to permit fabrication of the COS/MOS devices.

Experiments were performed to finalize the structure of the composite SiO_2/Si_3N_4 gate dielectric required for trimetal COS/MOS integrated circuits. Circuits were fabricated with 200 Å and 400 Å Si_3N_4 layers on 900 Å and 800 Å SiO_2 layers, respectively, and subjected to bias life testing. The results are summarized in Table V-11. Based on these data, a dielectric of 900 Å of SiO_2 and 200 Å of Si_3N_4 was chosen for the COS/MOS circuits.

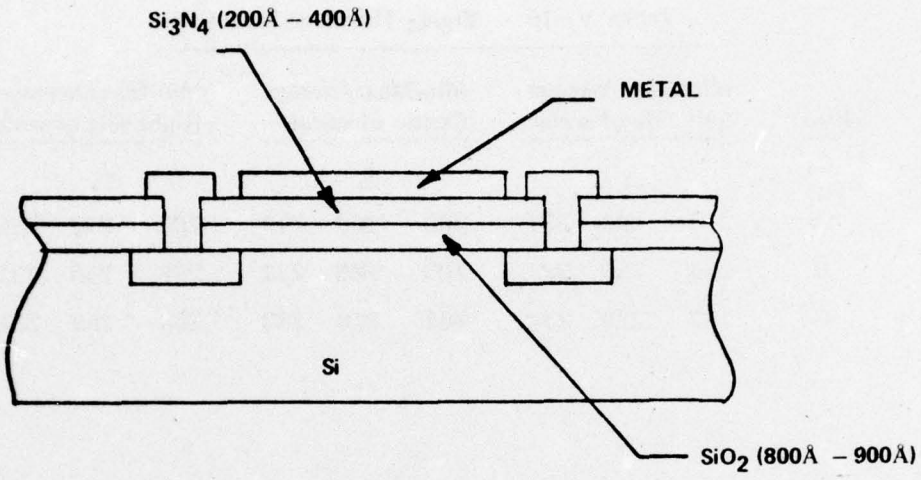
Table V–10 – Si_3N_4 Thickness Variations

Run	Min/Max/Average Left side of wafer			Min/Max/Average Center of wafer			Min/Max/Average Right side of wafer		
	Å			Å			Å		
A	210	244	221	200	260	219	200	277	235
B	208	250	221	200	265	231	208	250	231
C	193	273	234	201	258	233	208	258	234

Table V - 11 – COS/MOS Gate Dielectric

Si_3N_4 Thickness Evaluation

Basic Structure Under Evaluation



Operating Life Data for Negative Bias

Bias/Temperature Conditions	Duration (Hours)	Silicon Nitride Thickness			
		200Å		400Å	
		ΔVTN	ΔVTP	ΔVTN	ΔVTP
125°C – 12 V	1000	+0.12	–0.12	–	–
	2000	+0.13	–0.14	–	–
150°C – 12 V	168	+0.10	+0.12	+0.26	–0.22

Operating-Life Data for Positive Gate Bias Show No Change

Conclusions

1. Stable Trimetal COS/MOS Devices can be Fabricated.
2. Stability Improves with Thinner Si_3N_4 Layers.
3. The Mechanism for Instability is Consistent with Electron Conduction Through the Si_3N_4 Resulting in Interface Charging.

3. Silicon Nitride Plasma Etch Evaluation

Conventional wet chemical processing techniques for etching Si_3N_4 involve the use of phosphoric acid at a temperature of 180°C. Since photoresist materials will not withstand etching at this temperature, a chemically vapor deposited (CVD) SiO_2 film is used as the etch mask, further complicating the process. Plasma etching offers a simplified, cost reduced alternative to this system, as shown in Table V-12.

The effects of plasma etching on the SiO_2/Si_3N_4 dielectric films have been investigated by means of capacitance voltage-bias temperature tests. These results are shown in Fig. V-11. The figure shows that a 530°C, 20-minute anneal in forming gas appears to be sufficient to eliminate charge induced during the etching process.

Device wafers of types 5420 and CA741 have been fabricated using plasma Si_3N_4 etching. Circuit-probe yields and parameter distributions equivalent to those achieved with chemical etching techniques were achieved on type 5420. The CA741 exhibited depressed circuit-probe yields when subjected to plasma etching. Analysis has indicated some degradation in low current β, a parameter to which this circuit is sensitive. Processing techniques to correct this problem are under investigation while wet chemical etching remains the standard Si_3N_4 etching process.

4. PtI-Ti-PtII Metallization

Trimetal MOS devices have, in the past, been fabricated by means of the titanium palladium gold system. The reason for this is the sensitivity of MOS devices to sputter damage during the Ti/Pt deposition process used for bipolar devices and the

Table V–12 – Chemical vs Plasma Etch Process Comparison

Chemical Etch	Plasma Etch
1. Deposit SiO_2	1. Apply Photoresist
2. Apply Photoresist	2. Etch Si_3N_4
3. Etch	3. Etch SiO_2
4. Remove Photoresist	4. Remove Photoresist
5. Etch Si_3N_4	
6. Etch Top Layer SiO_2 and Contacts	

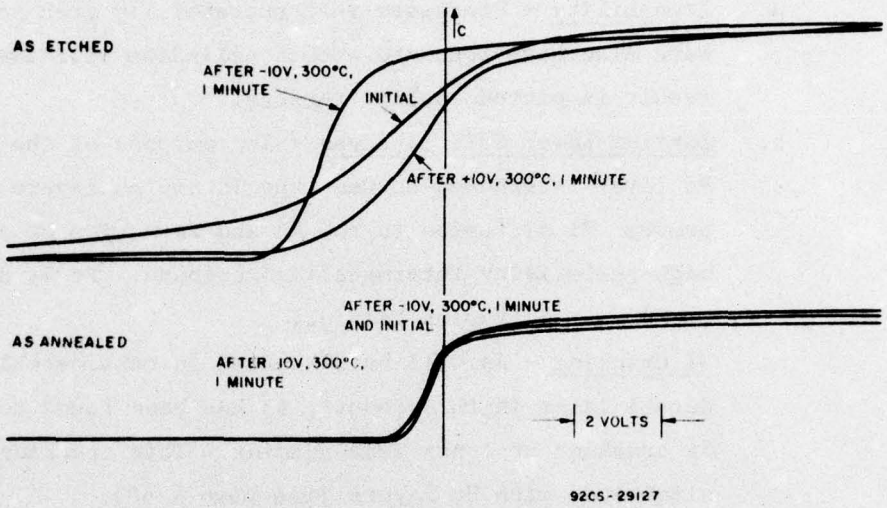


Fig. V-11 Capacitance voltage-bias temperature tests after Si_3N_4 plasma etch and after 530°C 20-minute forming-gas anneal.

high boiling point of platinum, which precludes its use in an evaporation system. It has been found that palladium has the following three major disadvantages as a constituent of a trimetal system, as compared to platinum:

a. Etchability - Processes that successfully etch palladium have also been found to attack palladium silicide; the result is pitted contact regions.
b. Barrier Layer Effectiveness - The purpose of the Pt or Pd layer interposed between the Ti and Au layers is to prevent Ti diffusion to the Au and formation of a relatively high-resistivity intermetallic compound. Pt is superior to Pd as a diffusion barrier.
c. Si Cracking - As will be discussed in considerable detail later in this report, Pd has been found to induce Si cracking at inner lead bonding. This cracking is eliminated with Pt layers (See page V-68).

Furthermore, the successful application of the Ti-Pt-Au metal system to MOS devices would result in a single metallurgical system for all devices in manufacturing, thereby reducing process proliferation and minimizing capital investment.

Magnetron sputtering has been investigated as a technique for the deposition of Ti and Pt layers without the damage normally associated with conventional dc or rf sputtering processes. A Model 901 Materials Research Corporation Planar Magnetron Sputtering System was used for this work.

The results of capacitance-voltage bias temperature (CVBT) testing of a magnetron-sputtered Ti film, as deposited, are shown in Fig. V-12. These curves show an abnormal slope as well as a negative-bias temperature-stress instability. After a 320°C forming gas (90% N_2, 10% H_2) anneal, however, the sputter-induced damage was eliminated, as shown in Fig. V-13.

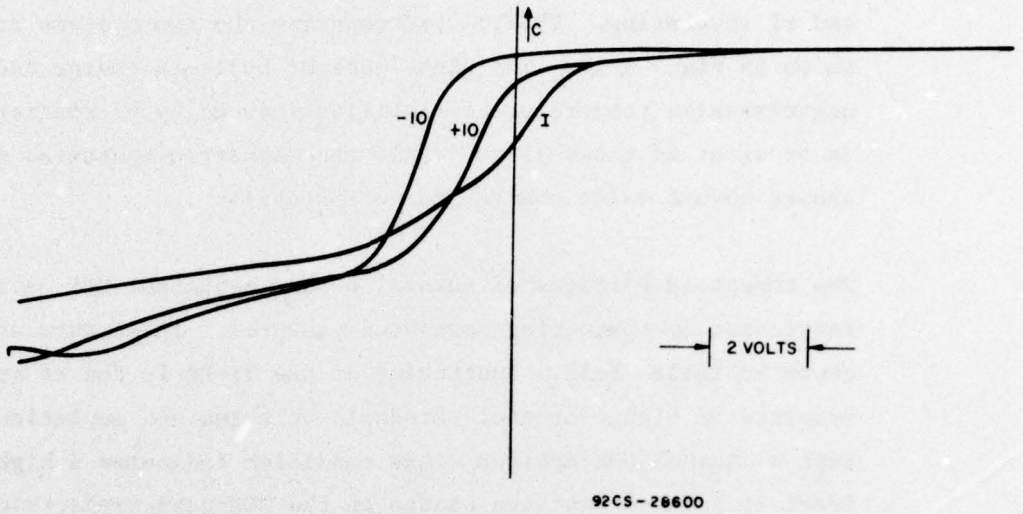


Fig. V-12 Capacitance voltage bias temperature test, magnetron sputtered Ti, unannealed.

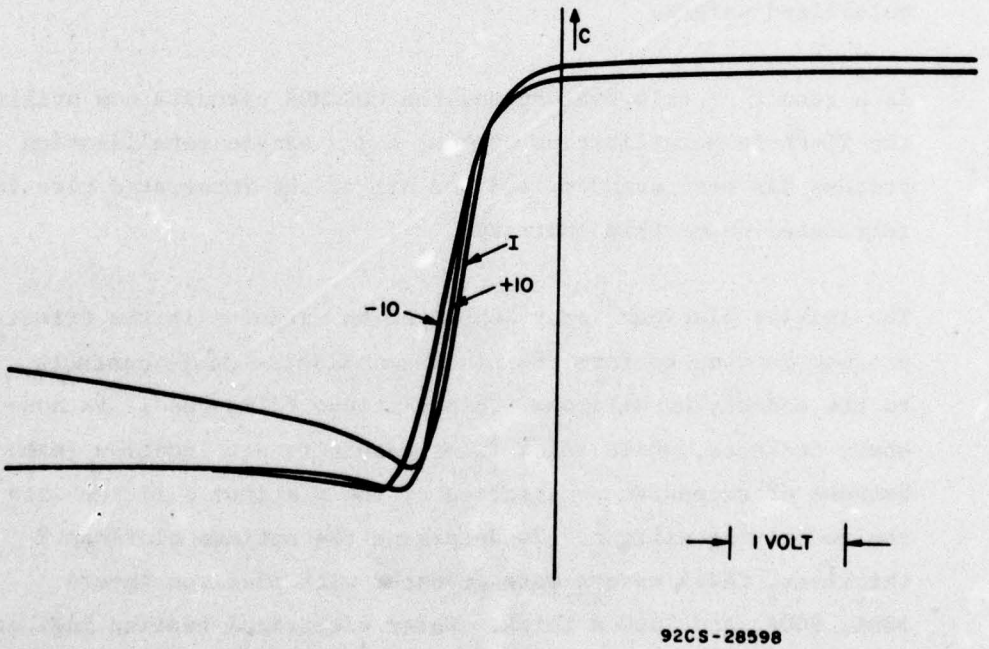


Fig. V-13 Capacitance voltage bias temperature test, magnetron sputtered Ti-Pt after 320°C 16 hour anneal in forming gas.

Samples of the CD4012B have been fabricated with both magnetron and rf sputtering. CVBT plots comparing the two systems are shown in Fig. V-14. The high level of built-in charge and negative-bias temperature instability induced by rf sputtering is apparent in these plots, while the magnetron-sputtered sample showed normal oxide charge and no instability.

The threshold voltages of several p- and n-channel MOS devices fabricated by sputtering have been measured. These data are shown in Table V-13. Sputtering of the Ti-Pt in the rf system resulted in high p-channel threshold voltages and depletion type n-channel MOS devices; this condition indicates a high level of induced positive charge in the MOS gate dielectric. MOS transistor parameters for the magnetron-sputtered samples were normal. Electrical testing of trimetal COS/MOS wafers fabricated with the magnetron-sputtered Ti-Pt wafers has provided yields equivalent to those obtained with conventional aluminum metallized wafers.

As a result of this evaluation, the COS/MOS circuits now utilize the Ti-Pt-Au metallization system, and a single metallization process has been standardized for all of the integrated circuits fabricated under this contract.

The initial platinum layer deposited on circuits in the trimetal process is used to form the platinum silicide ohmic contacts to the underlying silicon. Thin platinum films result in non-ohmic contacts, while thick films result in p-n junction leakage because of excessive penetration of the platinum silicide into the underlying silicon. To determine the optimum platinum I thickness, CA741 wafers were prepared with platinum layers 500Å, 800Å, and 1400 Å thick. Wafer electrical testing indicated that yields are adversely affected by increased thickness of platinum. As a result, the trimetal process has been standardized with a platinum I thickness of 500Å to 700 Å.

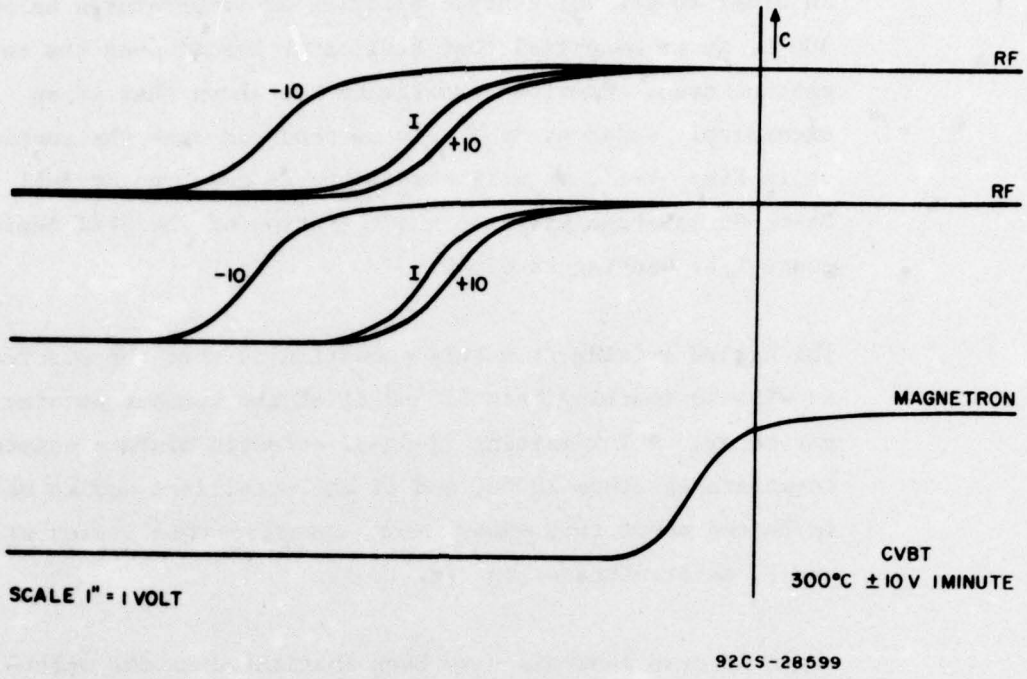


Fig. V-14 Capacitance voltage bias temperature test, magnetron versus rf sputtering, after 16 hour anneal in forming gas.

Table V–13 – Threshold – Voltage Comparison

Sample	Ti/Pt-RF Sputtered		Ti/Pt-DC Magnetron Sputtered	
	V_{TP} (Volts)	V_{TN} (Volts)	V_{TP} (Volts)	V_{TN} (Volts)
1	4.06	Depletion	1.58	1.60
2	4.5	"	1.52	1.68
3	4.1	"	1.36	1.66
4	4.0	"	1.32	1.56

In order to prevent contact alloying at temperatures below 300°C, it is essential that PtSi cover the Si over the entire contact area. Previous experience has shown that if an excessively undercut Si_3N_4 lip is produced over the contact, as in Fig. V-15, it will shadow the Si and prevent full Pt-to-Si coverage prior to the formation of the PtSi ohmic contact by heating to 620°C.

The hazard arising from this condition is that the electroplated Au will be touching both Si and Ti at the contact opening perimeter. A low melting Ti-Au-Si eutectic mixture exists at temperatures above 280°C, and if the metallized device wafer is heated above this temperature, catastrophic alloying will occur, as illustrated in Fig. V-16.

Rigid process controls have been instituted in the wafer-processing area to avoid this unacceptable alloying by minimizing the Si_3N_4 lip undercutting and thereby assuring that the PtSi ohmic contact fully overlaps the underlying Si. As a definitive control, each wafer is exposed to a temperature of 320°C for 16 hours, following which failing wafers are readily identified by discolored Au areas over the contacts. Trimetal wafer processing has incorporated this critical 320°C heat-treatment since its inception, resulting in only random failed wafers. The structure of an acceptable ohmic contact is shown in Fig. V-17.

The sputtered titanium film provides adherence between the silicon nitride film and the subsequent Pt and Au layers. Ease of etching and continuity are the prime requirements placed on this film. Film thicknesses of 1000 Å to 1200 Å have been found to be optimum for these purposes.

The function of the platinum II layer is to provide a barrier between the previously deposited titanium and the gold which is subsequently electroplated. It is imperative that diffusion

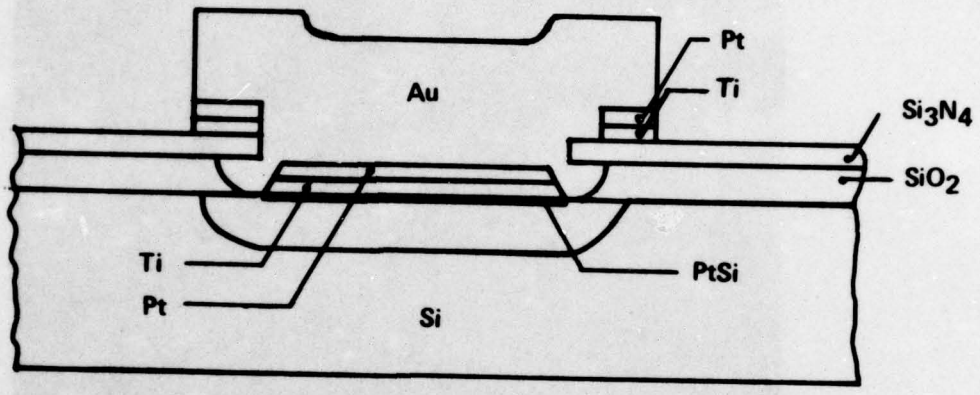


Fig. V–15 Inadequate PtSi formation resulting from excessive Si_3N_4 lip.

Fig. V – 16 Bevel-lapped cross section. Alloying at 280°C in unacceptably metallized device.

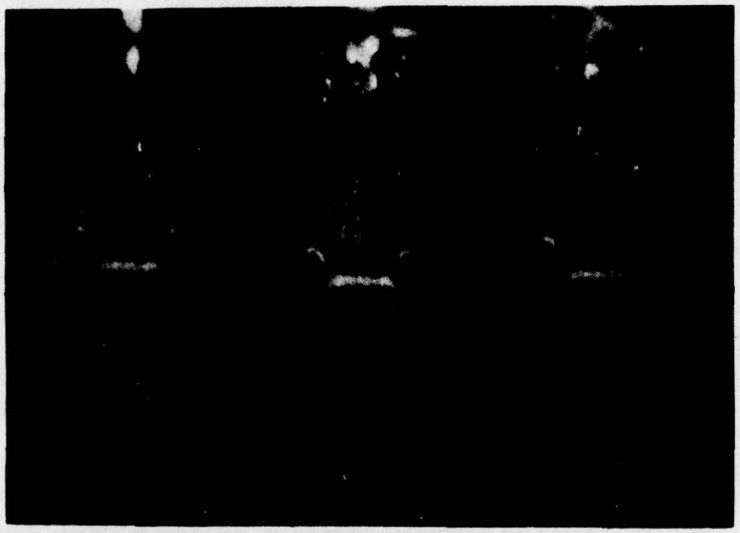


Fig. V–17 Bevel-lapped cross section. Acceptable trimetal structure following 320°C exposure.

between titanium and gold be prevented since it leads to the formation of a relatively high resistivity intermetallic compound. To determine the optimum thickness of the platinum, a series of CA741 wafers were fabricated with 1500 Å, 2500 Å and 3500 Å platinum layers. These wafers were heated to a temperature of 400°C while under constant visual observation. No darkening or change in texture of the gold plating was observed, indicating that the minimum thickness evaluated, 1500 Å, is an effective diffusion barrier between titanium and gold.

5. Gold Interconnect Thickness Evaluation

The Au interconnect levels are electroplated into an opened photoresist configuration over defined Pt lines utilizing the underlying Ti as a conductive bus layer. This technique has proven extremely economical when compared to vacuum deposition processes requiring the wasteful subsequent removal of excess Au. Since the plating process deposits Au only where it is required to controlled thickness levels, maximum utilization of the deposited Au is obtained at a minimum cost.

The thickness of the plated gold interconnects has been investigated from the standpoint of oxide step coverage. Figs. V-18 and V-19 are 1000X SEM photographs of 1.5-micron and 2.5-micron thick gold metal runs, respectively, and show the excellent step coverage obtained with the 1.5-micron thickness. The reduction in thickness from the previously used 2.5-micron layers results in reduced mushrooming during plating, improved protective layer coverage, and increased wafer throughput. As a result of this evaluation, the gold interconnect thickness has been standardized at 1.5-micronson all circuits.

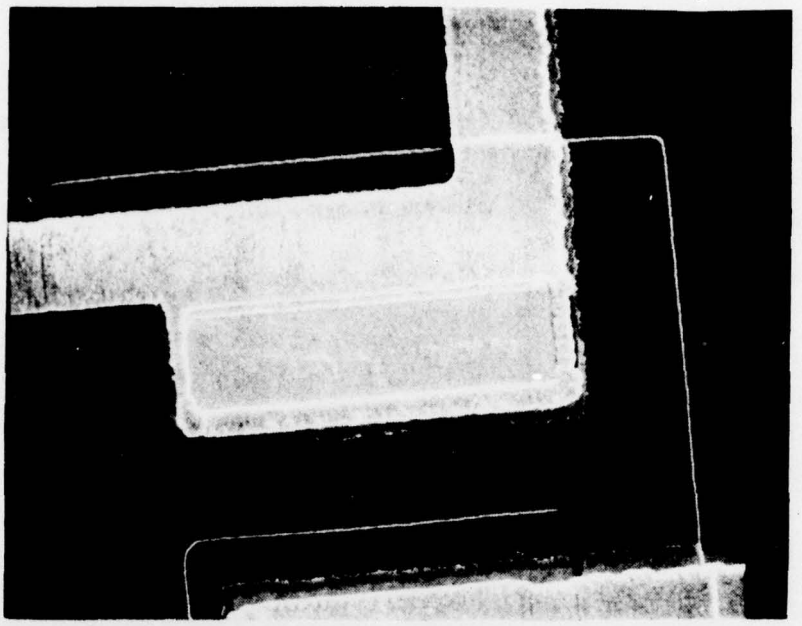


Fig. V-18 1.5-micron gold, 1000X SEM photograph of collector contact.

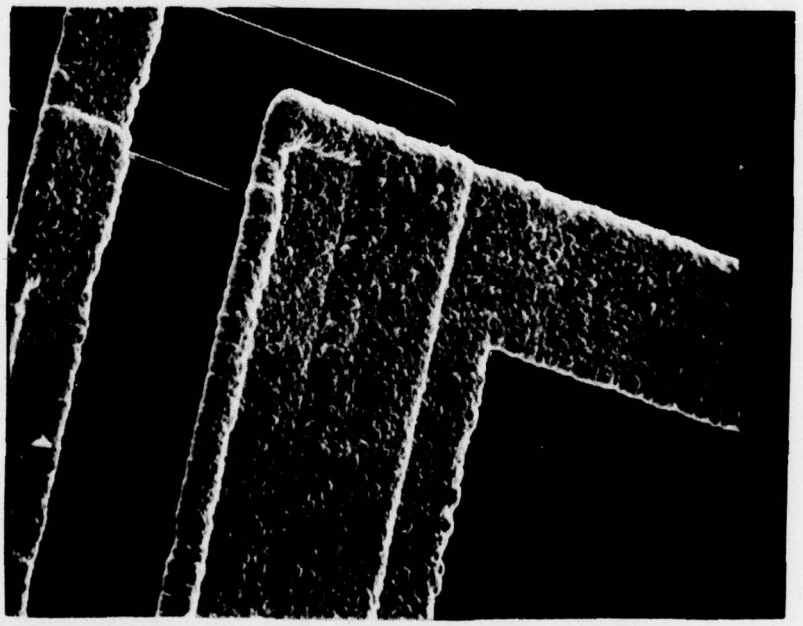


Fig. V-19 2.5-micron gold, 1000X SEM photograph of collector contact.

6. Bond Pad Height Evaluation

The assembly of integrated circuits using beam-tape bonding techniques requires elevated bond pads on the silicon wafers. Experimentally, it has been determined that bond pads in the order of 25 microns in height are required to assure sufficient clearance between the beam tape and wafer surface. Conventional wet photoresist techniques provide relatively thin masking films compared to the desired pad height. This situation results in bond pads that have a mushroom-shaped cross section, as shown in Fig. V-20, not entirely suitable for bonding. In order to provide bond pads of the proper height with a uniform cross section, a dry-film photoresist process has been developed. This photoresist is a negative working film 25 microns thick interposed between layers of mylar and polyolefin. Processing of this material to achieve the 25-micron-high bond pads is carried out as follows:

a. The dry-film photoresist is laminated to the integrated-circuit wafers by passing both materials through heated rollers. During this process, the backing material (polyolefin) is separated from the resist, permitting intimate contact between the dry film and underlying photoresist layers.
b. The bond-pad pattern is now aligned and exposed to the wafer as in a conventional photoresist process.
c. After removal of the mylar cover sheet, the dry film resist is spray-developed in a butyl acetate-toluene mixture to define the bond-pad areas.
d. The gold bond pads are plated to the desired thickness.
e. The photoresist is removed.

This process results in bond pads with uniform cross sections of the desired height as shown in Figs. V-21 and V-22.

Fig. V-20 Cross section of a Au bond pad plated by means of the wet photoresist process.

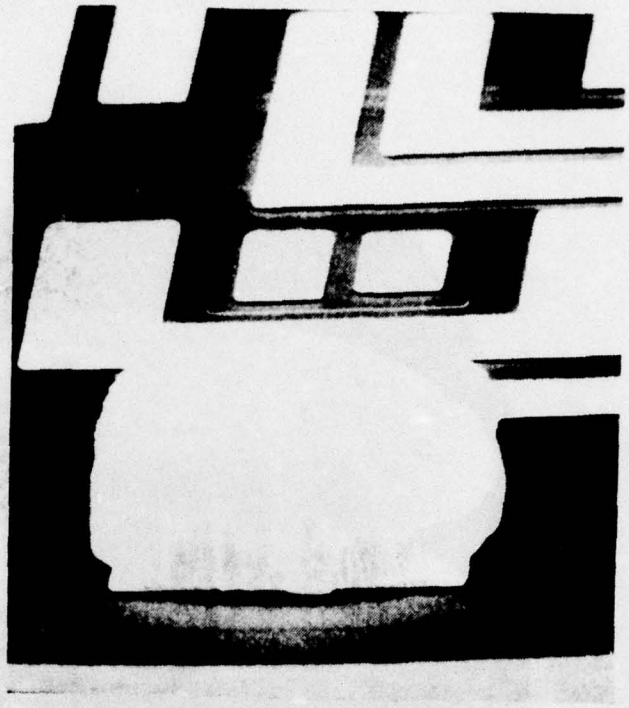


Fig. V-21 Plated gold bump.

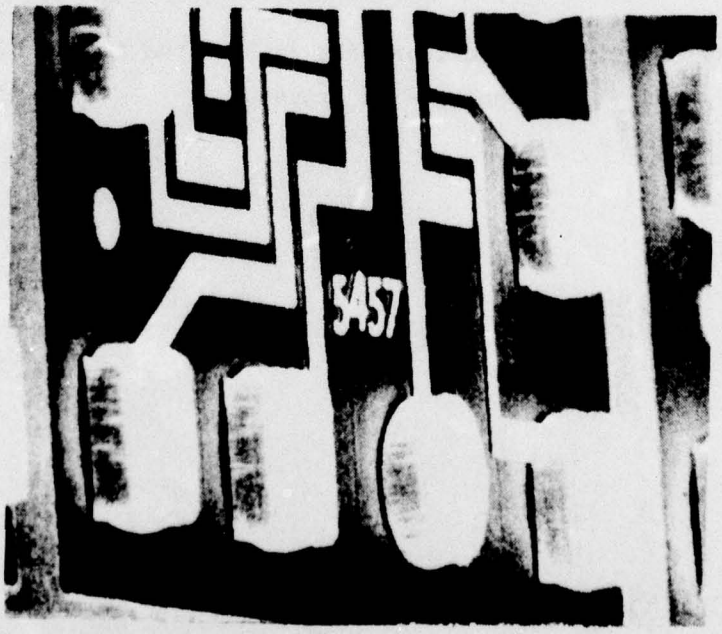


Fig. V-22 Wafer after gold-bump plating.

Variations in bond-bump heights between 0.0005-inch and 0.0015-inch have been investigated for optimization in terms of cost, ease of fabrication, and reliability considerations. An eventual decision was made to standardize the 0.001-inch bump height for the following reasons:

- The 0.0005-inch bump height is equivalent to the thickness of the beam-tape polymide support film. The undesirable possibility exists that the polyimide thickness may prevent adequate bump deformation during the inner lead thermocompression bonding.
- The 0.001-inch bump height precludes the eventuality described above. Additionally, as shown in the accompanying metallographic cross sections, it provides a safety margin, derived from its increased elevation, against the possibility of shorts to the edge of the chip or to the internal metallization.

  Fig. V-23 illustrates a normally aligned inner lead bond to a 0.001-inch-high bond bump. It will be noted that the deformation accompanying bonding causes the beam to lift away from the edge of the chip - at the left edge of the photomicrograph. Conversely, in Fig. V-24, a beam-to-bump bond is illustrated in which an overlong and misaligned finger extends inboard with respect to the bump. Although there is no edge-short hazard, it is apparent that the overhanging beam has been depressed close to the device metallization. The 0.001-inch-high bump provides an additional margin of safety in this area.
- The bumps are plated into a patterned, dry-film photoresist material requiring exposure and development. This material becomes more difficult to process as its thickness increases, and therefore the use of the 0.0015-inch-thick photoresist required for straight-sided 0.0015-inch-high bumps is considerably less desirable than a thinner resist film.

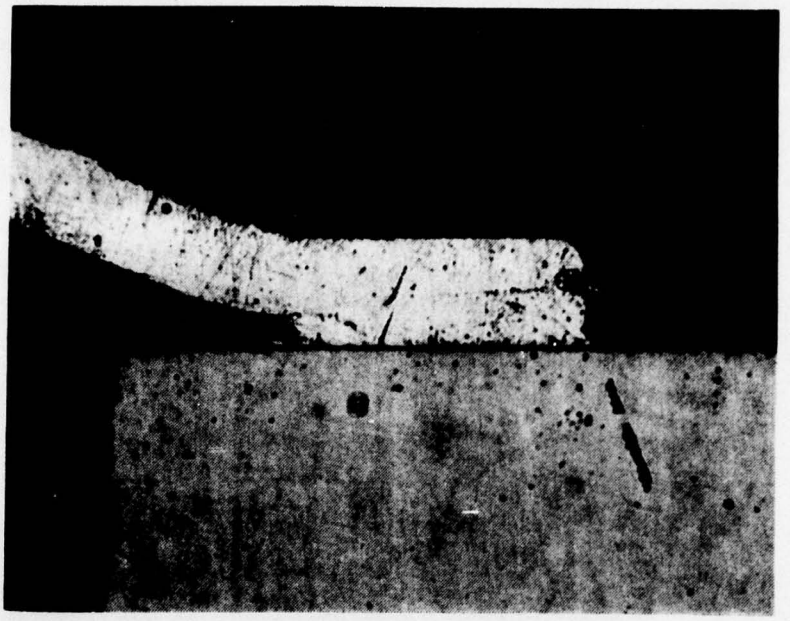


Fig. V- 23 Normal inner-lead bond, 400X.

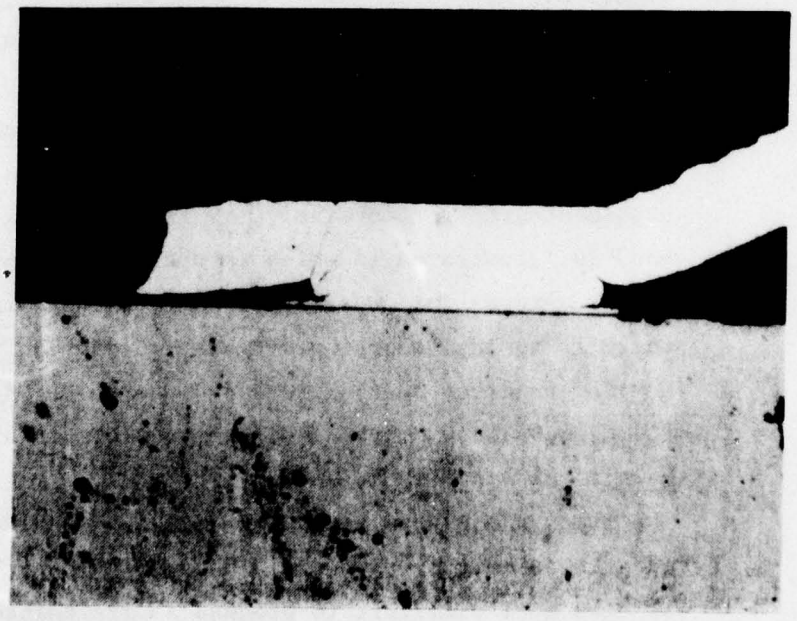


Fig. V- 24 Misaligned inner-lead bond, 400X.

- The factor of Au costs favors the lowest feasible bump height compatible with device reliability. The 0.001-inch-high bump represents an optimal choice in this area.

7. Sputter-Etch Process Evaluation

The sputter-etch process is a technique that eliminates a photolithographic step from the trimetal process, provides line-to-line (Pt to Au) registration, and improved gold plating uniformity over that achievable with the chemical etching process. A comparison of the two processes is shown in Table V-14.

Results achieved to date on COS/MOS circuits have shown that sputter etch and chemical etch processes provide equivalent yields. No parameter degradation occurs during sputter etching and the capacitance voltage-bias temperature plots show no instability, Fig. V-25.

The sputter-etching process has also been applied to bipolar circuits, but with limited success. The process has been observed to leave residual platinum filaments at oxide steps; the filaments cause electrical shorts. SEM photographs of these filaments are shown in Figs. V-26 and V-27.

The source of these filaments is related to the steepness of the oxide-step slopes on integrated circuits. The COS/MOS circuits utilize sloped-oxide etching techniques that result in tapered-oxide steps that permit complete Pt removal on sputter etching. Tests of sputter etching on bipolar circuits have indicated that residual platinum filaments are found at the edges of the relatively steep oxide steps as the Pt removal rate falls off close to these steps. The Pt filaments may be eliminated on bipolar devices by modification of the sputter-

Table V-14 - Pt Chemical vs Sputter Etch Process Comparison

CHEMICAL ETCHING	SPUTTER ETCHING
1. Sputter Ti/Pt	1. Sputter Ti/Pt
2. Pt Photoresist	2. Au 1 Photoresist
3. Pt Etch	3. Au 1 Plate
4. Photoremoval	4. Au 2 Photoresist
5. Au 1 Photoresist	5. Au 2 Plate
6. Au 1 Plate	6. Photoremoval
7. Au 2 Photoresist	7. Sputter Etch Pt
8. Au 2 Plate	8. Ti Etch
9. Photoremoval	
10. Ti Etch	

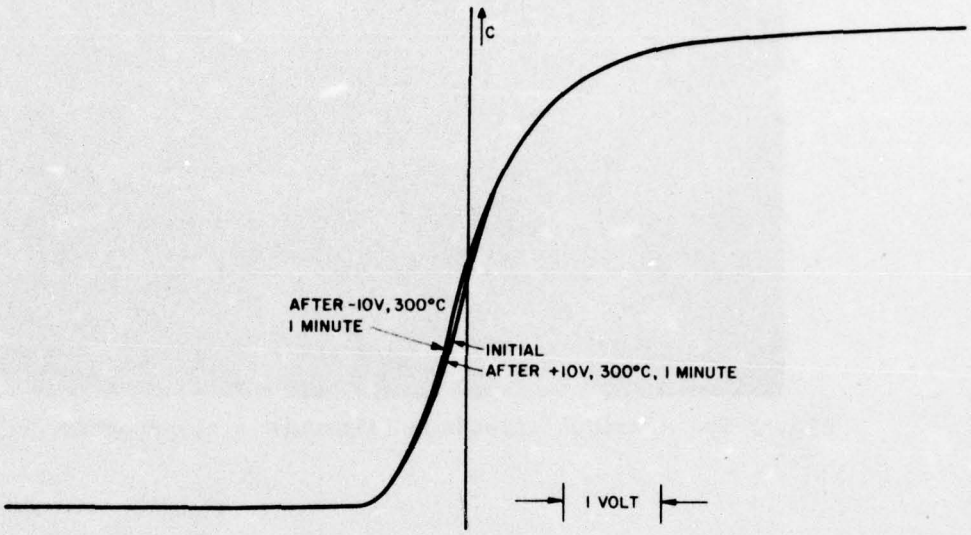


Fig. V-25 Capacitance voltage-bias temperature test after sputter etch.

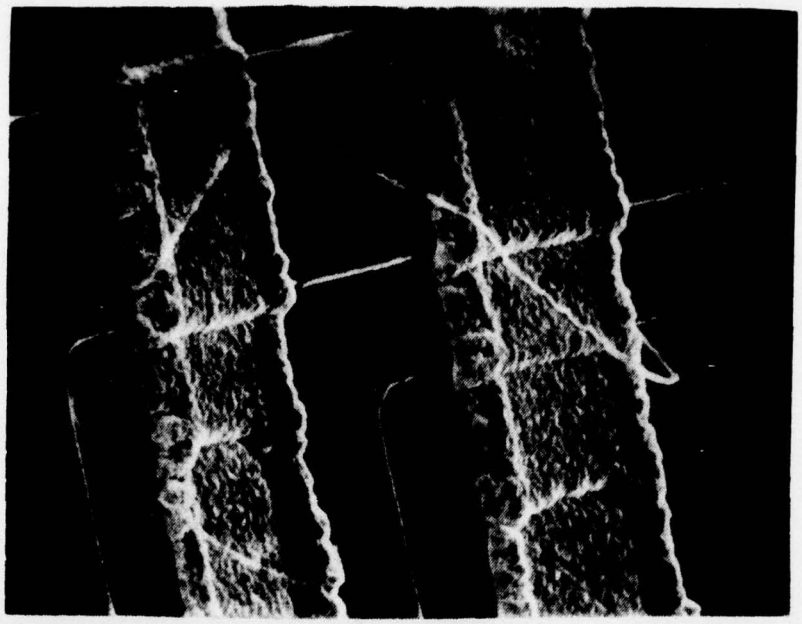


Fig. V-26 Residual platinum filaments after sputter etching.

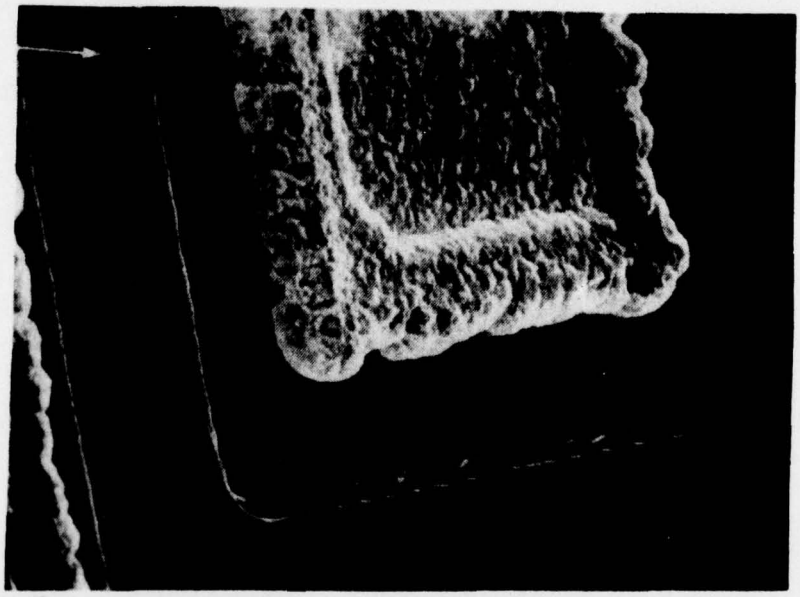


Fig. V-27 Residual platinum filaments after sputter etching.

etch conditions. While this work is in progress, chemical Pt etching continues to be the standard trimetal process.

8. Post-Ti Etch Bake Evaluation

Subsequent to the titanium etch process, trimetal wafers are baked for a period of sixteen hours at 325°C. The absence of darkened gold plating after this bake indicates the effectiveness of the platinum layer as a barrier against titanium-gold intermetallic diffusion. To insure that this procedure does not adversely affect the titanium-silicon nitride bond, units were completed through inner-lead automated bonding and pull-strength tested. It was found that in all cases the failure mode was lead breaks, not bond-pad lifts, verifying the basic integrity of the Ti-Si_3N_4 interface.

9. Silicon Nitride Overcoat Technology

A potentially serious failure mode that can occur with gold-surfaced semiconductor metallization is the formation of electroplated migrative short circuits. The prerequisite for this phenomenon is the presence of a contaminated film of moisture containing a dissolved ionic contaminant, such as chlorine, between oppositely biased metallization stripes. Shorting caused by the electroplating phenomenon is eliminated by deposition of a dielectric protective layer over the wafer surface. Techniques have been developed on commercially available equipment (AMI Plasma Reactor) for depositing a silicon nitride film layer to overcoat the metallization and the junction-sealing SiO_2/Si_3N_4 films. This final Si_3N_4 layer is deposited at temperatures between 250°C and 300°C in an rf-induced plasma that is compatible with both bipolar and COS/MOS integrated circuits. Tests to assure that the deposited films are a true electroplating barrier have been devised and are described below.

Integrity Test - Gold-metallized wafers coated with a Si_3N_4 film are immersed in aqua regia for 2 minutes at 100°C. Lack of integrity is indicated by attack of the gold metal runs. An SEM photograph of a cross sectioned conductor is shown in Fig. V-28. The photo indicates the excellent conformity and integrity achieved with rf plasma-deposited Si_3N_4.

Adherence Test - Wafers are subjected to a "Scotch" tape peel test immediately after deposition and after immersion in water for 16 hours. The Si_3N_4 film does not separate from the underlying surface at any point, thereby attesting to the superb adherence of plasma deposited Si_3N_4 over Au.

Thermal Shock Test - Devices are subjected to automated inner lead bonding with a bond tool temperature of 500°C. The absence of cracking and blistering over large-area Au surfaces indicates the ability of these films to withstand thermal shock.

Film Stress Test - Many of the properties of deposited films are related to the stress induced in these layers during deposition. A convenient method for measuring this stress is to deposit the film on a thin circular substrate with known physical characteristics and to measure the resultant bow in the substrate upon cooling to room temperature. The stress may then be calculated from the equation derived by Glang[1]. Typically:

$$\sigma = \frac{\delta}{r^2} \quad \frac{Es}{3(1-v)} \quad \frac{ts^2}{tf}$$

where σ = Stress (dynes/cm^2)

δ = Deflection of disc (cm)

v = Poisson's ratio of substrate

E = Young's modulus of substrate

tf = Film thickness (cm)

ts = Substrate thickness (cm)

r = Radius of disc (cm)

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[1] Glang, R., Holmwood, R., Rosenfield, R., Rev. Sci. Instr. 36, 7 (1965).

Fig. V-28 Cross sectioned conductor with rf plasma-deposited Si_3N_4 overcoat.

A compressive stress of approximately 4.9×10^{-9} dynes/cm^2 is attained. This figure compares favorably to the value of 3×10^9 dynes/cm^2 in tension obtained with CVD/PSG protective dielectric films.

Thickness - It has been determined that Si_3N_4 film thicknesses in the range between 10k Å and 12K Å will effectively seal over the 15-kÅ Au interconnect steps. Thickness measurement is performed on a Beckman DK2 recording spectrophotometer or its equivalent. Deposition rates of approximately 200 Å per minute are obtained reproducibly, the AMI reactor yielding 25 deposited 3-inch-diameter wafers per hour.

Etch Rate - The etch rate of the deposited film is measured in room temperature buffered HF (15% HF, 85% NH_4F), and serves as an indication of the purity of Si_3N_4. Etch rates of 250 Å per minute are typically associated with uniformly deposited Si_3N_4 layers. Etch rates lower than this indicate a Si-rich deposited film while a higher etch rate denotes excessive SiO_2 contamination. Since the Si_3N_4 is a product of a complex pressure- and temperature-dependent reaction:

$$SiH_4 + NH_3 + N_2 \rightarrow Si_3N_4$$

it is essential that the etch rate be monitored continuously and process control limits be established at the 250 Å ± 25 Å per minute rate.

Refractive Index - An additional control over the Si_3N_4 film is related to the index of refraction of the dielectric. Consistently, films with refractive indexes between 2.0 to 2.2 are obtained and perform excellently as overcoating layers.

Electroplating Test - The final test to insure the integrity of the film as an electroplating barrier is to assemble units in open DIC packages and subject them to 85°C/85% RH bias life testing. The period of time required to form electroplated shorts is the ultimate indicator of the film's integrity. Devices

have been subjectd to 250 hours of this test without failures. Testing is continuing. In previous tests, devices overcoated with chemically vapor deposited phosphorus silicate glass have exhibited a 40 percent failure rate at 140 hours; devices without overcoat protection generally fail within 48 hours.

It has been demonstrated conclusively that a commercially available procedure is available for Si_3N_4 dielectric protection of the Au lines in biased humid atmospheres. This overcoating is superior to the CVD/PSG in the following respects:

- Si_3N_4 provides superior conformity and adherence.
- Si_3N_4 will not absorb moisture and lose adherence. CVD/PSG loses adherence on exposure to moisture.
- Si_3N_4 provides protection against electroplated short circuits in open packages. By contrast, the CVD/PSG only performs well in this respect when encased by the compressive stresses provided by the epoxy molding compounds used for plastic packages.

Inasmuch as Si_3N_4 coated trimetal devices can be operated in open packages for prolonged periods without failure, application to hybrid multichip circuitry in non-hermetic packages has become extremely attractive. Low-cost substrates populated with proven hermetically sealed devices is now a near-term feasibility.

D. Assembly Technology

1. Wafer Preparation

To prepare a completed trimetal wafer for automated assembly, several additional processing steps are required, as delineated below and in Fig. V-29.

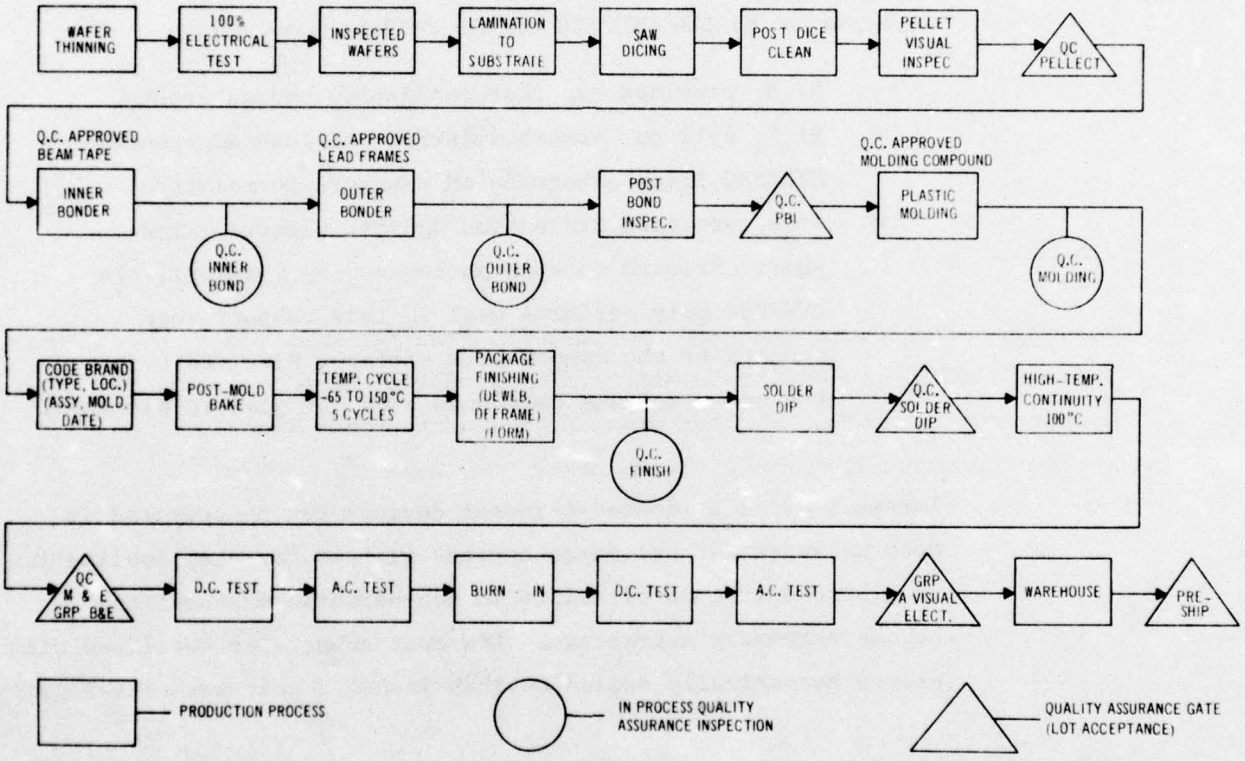

Fig. V-29 Assembly flowchart.

Wafer Thinning - To facilitate chip separation the wafers are back lapped to a finished thickness of 0.006 to 0.008 inch.
Electrical Test - Wafers are 100 percent electrical tested to eliminate chips that fail electrical specifications.
Lamination - The tested wafers are laminated to a supportive substrate through the medium of a paraffin based wax.
Sawing - The chips are separated by sawing entirely through the silicon wafer. At this point in the process, the substrate maintains the integrity of the chip matrix for inner-lead bonding.
Cleaning - After sawing, the chip matrix is cleaned and visually inspected for mechanical defects. Chips exhibiting such defects are identified with an ink dot to preclude their assembly into finished devices.

2. Beam Tape

Material - The beam tapes are constructed by laminating a layer of 0.0014-inch-thick Cu with a film of 0.0005-inch supporting polyimide. Configuration of the pattern involves photodefinition and etching of the Cu and polyimide to produce the required number of beams projecting into a central hole in the support film; this arrangement is illustrated in Fig. V-30.

It was determined early in the program that the originally proposed tape construction involving Au plating over the Cu beams gave rise to difficulty in bonding to the device bond pads. Examination of the beam structure disclosed that there was considerable variation in the thickness of the intermediate barrier layer of Ni that provided protection against Cu to Au interdiffusion at elevated temperatures. Where the Ni was found to exceed 50 microinches in thickness, poor bond strengths resulted. This condition is illustrated in Fig. V-31.

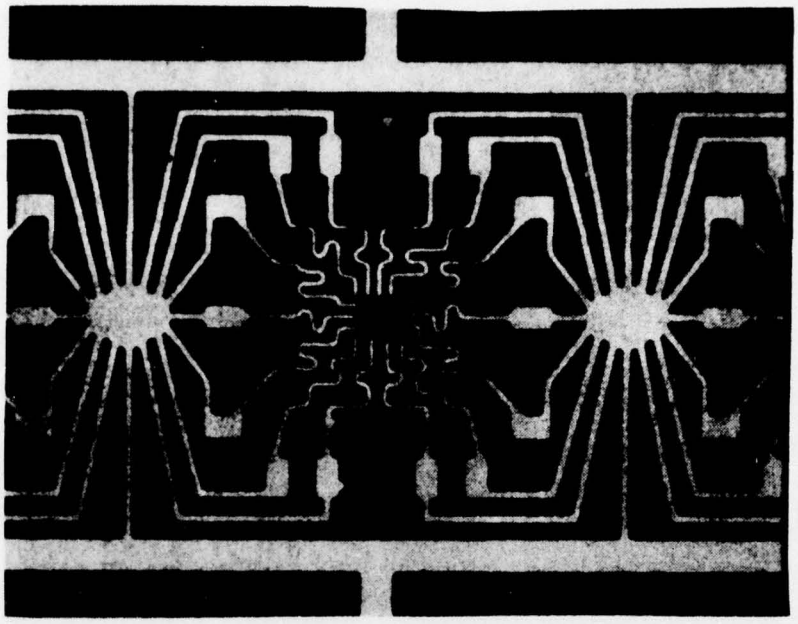

Fig. V-30 Beam Tape pattern.

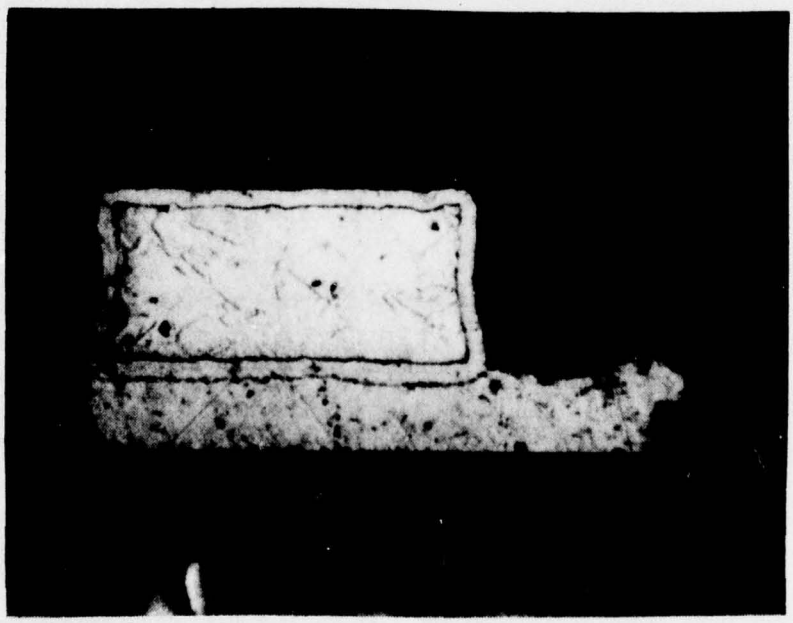

Fig. V-31 Cross section of low strength bond. (800X)

A solution to this problem, primarily for reasons of achieving low cost, is to eliminate both the Au and Ni. Results with bare Cu to Au bump bonding have been excellent, with the normal 40 to 50 gram bond strengths being maintained. As indicated in Fig. V-32, prolonged exposure at 150°C causes no loss of bond strength.

At temperatures in excess of 200°C, strength deterioration is noted. This has been related to the formation of the intermetallic compound Cu_3Au as the bonded Cu beam and Au bump interdiffuse in greater quantities at increasingly elevated temperatures. This is shown metallographically in Fig. V-33, which is a bevel-lapped cross section of an inner-lead bond following 200°C exposure for 500 hours.

The Cu/Au system is characterized by a complete lack of the Kirkendall void formation and electrochemical corrosion associated with Al/Au alloys and, as a result, confidence is high in the inherent reliability of Cu beam tapes.

The Cu beam tape is specified to be 40 DPH microhardness. This is an optimum value between the higher value desired for beam tape fabrication handling facility and the generally softer value desired for thermocompression bonding. The Cu hardness is a function both of its original value and of the softening effect of the heating required for the polyimide support film polymerization. Further modification of this hardness is provided by the thermocompression bond and by polymerization of the epoxy molding compound. The result is that the Cu beam is essentially fully annealed in the final DIP package as a consequence of the several processing heat treatments. Fig. V-34 illustrates the diamond indentations along a beam cross section indicating little change in microhardness along the beam.

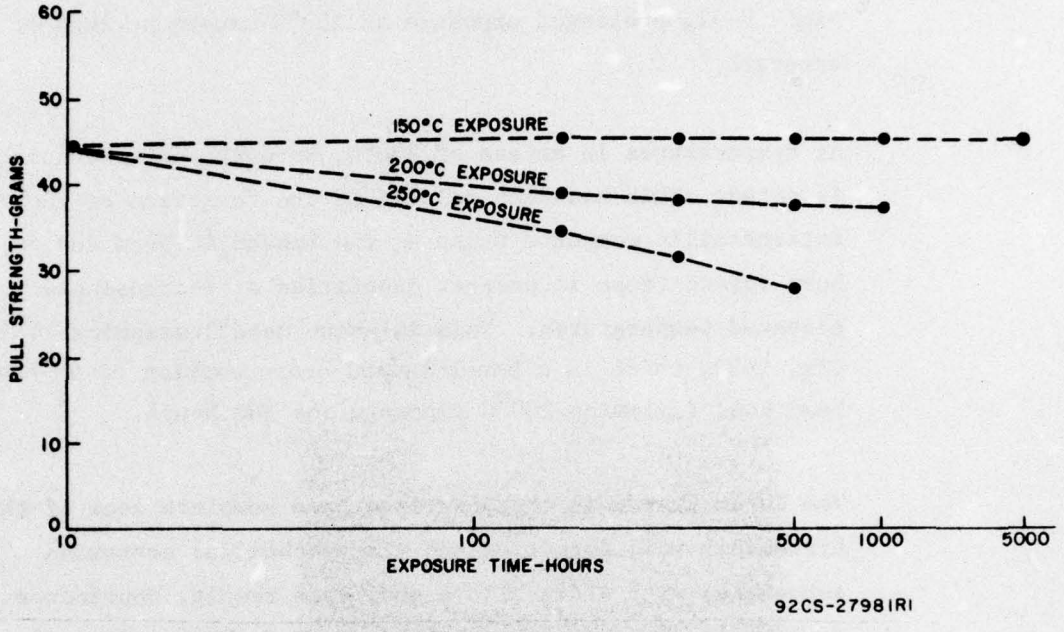

Fig. V-32 Bond strength of copper beams to gold bumps.

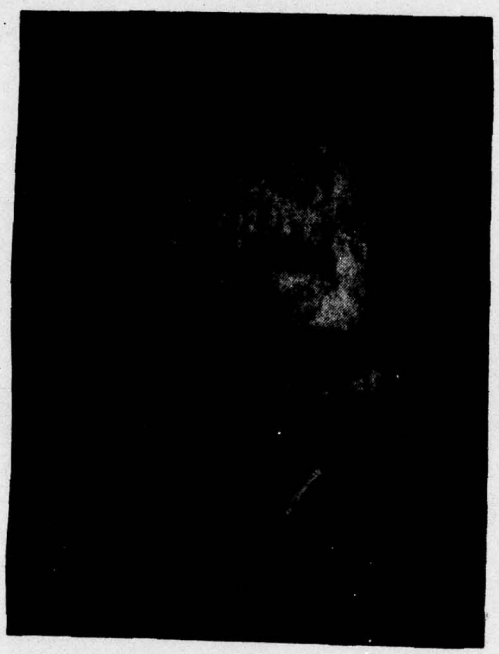

Fig. V-33 Bevel-lapped cross section of Cu beam-to-gold bump. Cu_3Au appears as dark intermediate area following 200°C exposure.

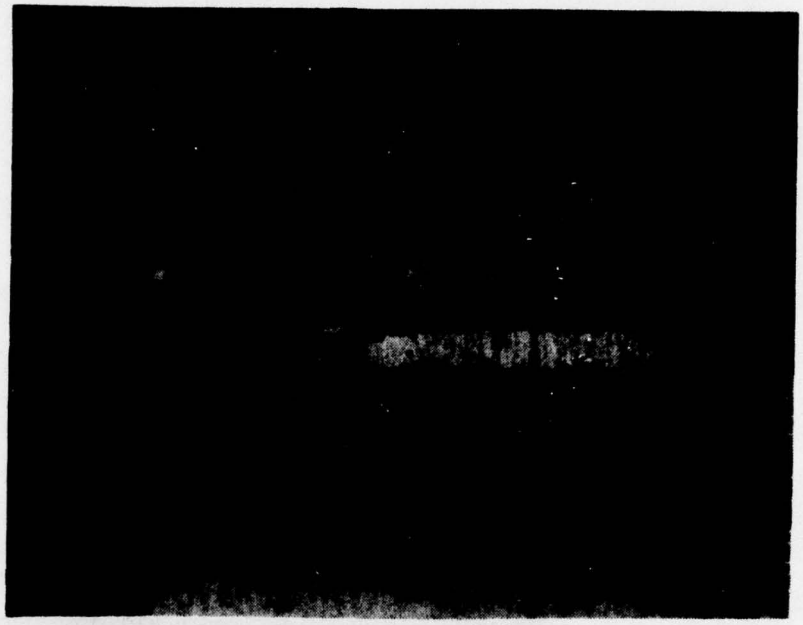

Fig. V-34 Cross section of copper beam showing uniform microhardness indentations.

Design - The design of the patterned Cu beam tapes is conditioned by requirements of stress relief, thermal conductivity, bond-pad spacing and position, and by the photochemical milling technology. It has been determined that the annealed condition of the Cu beam permits the use of beams of a width compatible with etching capability without an excessive increase in beam-induced structure stress at the bonds. This aspect is illustrated by the two contrasting beam-tape configurations in Figs. V-35 and V-36.

As a minimal design consideration, it is essential that the beams be aligned at the bond site in a direction perpendicular to the chip edge, and that whenever feasible, a change in beam direction be included between inner and outer bond locations to provide a measure of stress relief.

Computer-assisted design drawings were used for the layout for each device. This technique makes possible a consistent approach to the tape configuration and facilitates design modifications.

3. Inner Lead Bonding

Thermocompression bonding of beam tape to chip is accomplished on a Jade machine that provides rapid, accurate alignment between beams, device bumps, and heated tool. The latter is a precisely polished gem diamond that is heated to a temperature of 500°C. For bonds that are achieved in 0.3 seconds, the pressure applied is 113 grams per bond and the machine throughput ranges between 1500 and 2000 devices per hour.

Deformation of the beam and underlying bump are controlled carefully so that maximum strengths are achieved at each bond site. Evaluation of the inner-lead bond strength has been made

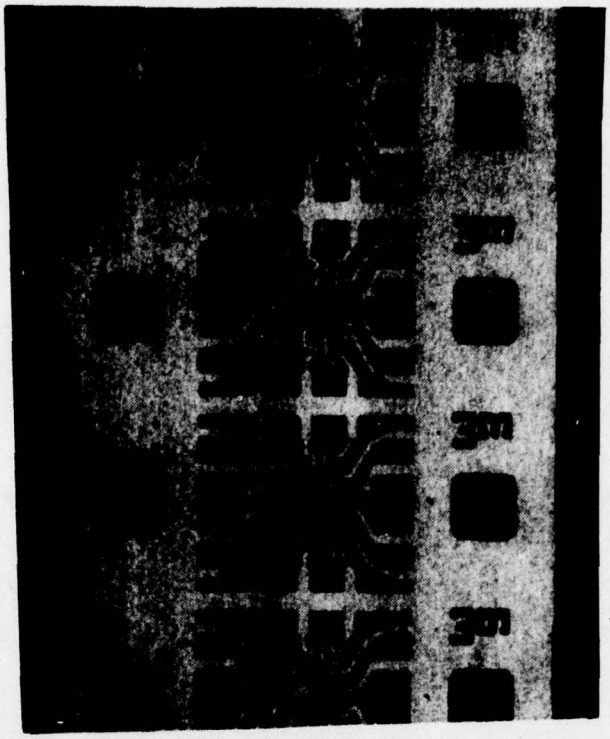

Fig. V-35 Early stress-relief design beam tape.

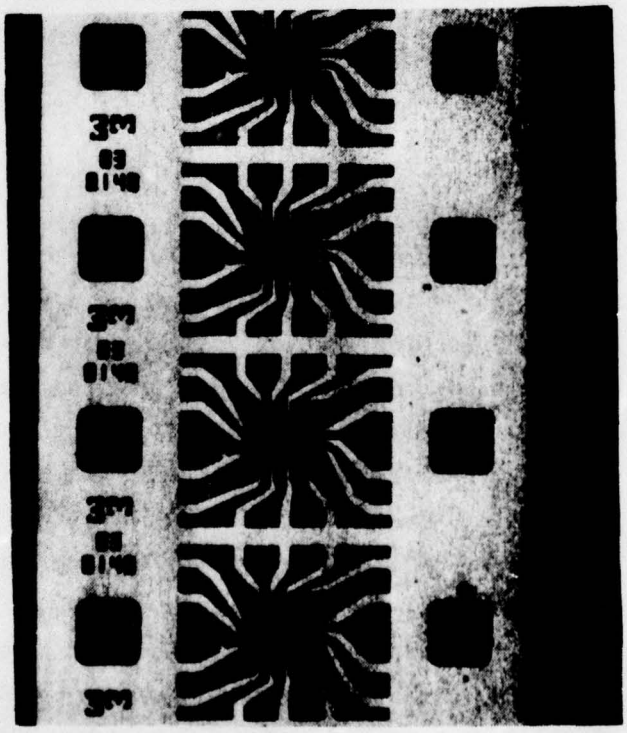

Fig. V-36 New type straight-line beam tape, CA741.

by pulling on individual beams and measuring the load required to break each beam. Pull strengths of 40-50 grams are associated with acceptable beam breaks. Unacceptably lower (20-40 gram) pull strengths are associated with anchor pad lifts, excessive beam deformation, or separation between beam and bump resulting from poor bonding.

A tester has been developed, as shown in Fig. V-37 on which force is applied to the device by a small tool that fits in the area surrounded by the bumps. The outer portion of the beams are clamped rigidly so that failure will occur in the beams or at the bonds.

Data obtained on devices bonded optimally indicate an overall maximum strength for 14-lead devices of 400 grams and of 500 grams for 16-lead devices. Acceptable bonding is indicated by the rupture of each beam at the minimum breaking strength. Unacceptable failures include separation of the bond pad from the device, cracking of the silicon, or separation between beam and bump. Fig V-38 describes the location of the pull-strength breaks. Fig. V-39 is a photograph of a tested 14-lead device with a breaking strength of 400 grams and 100-percent beam breaks. An unacceptable bond test, (totalling only 220 grams) is shown in Fig. V-40; only 2 beams broke, and the remaining bond-pad metallization separated from the device.

Silicon Cracking - An additional failure mode was observed, particularly on COS/MOS inner-lead bonds when Ti and Pd underlie the Au bump. Bond strength tests enable detachment of the bump from the device at low pull strengths as a result of cracking of the silicon underneath the bond-pad area. This type of breakage is illustrated in Fig. V-41. The figure shows a photo-micrograph of this type of cracking, which is conchoidal in nature, and an indication that high tensile stresses have been applied locally. This type of cracking has been completely eliminated by substitution of Ti-Pt-Au for Ti-Pd-Au.

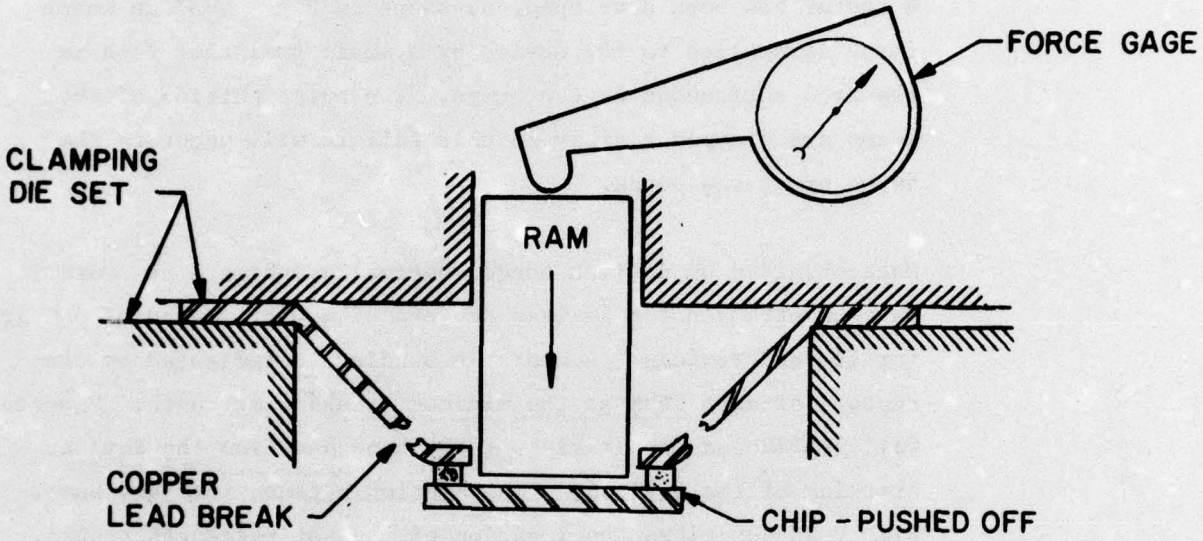

Fig. V-37 Inner-lead bond strength tester.

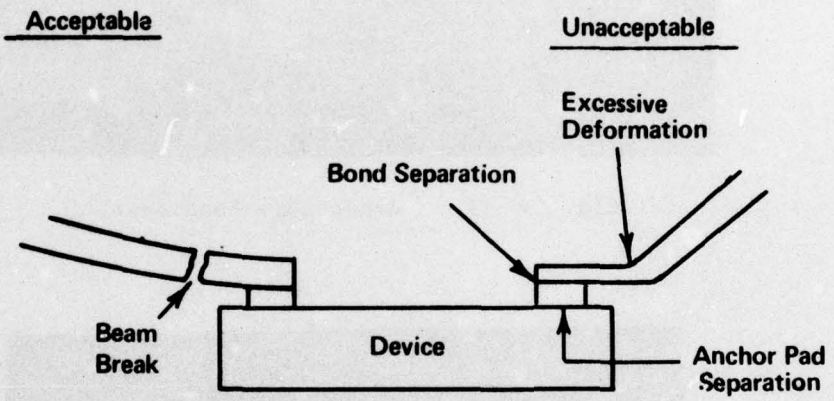

Fig. V-38 Pull-strength break locations.

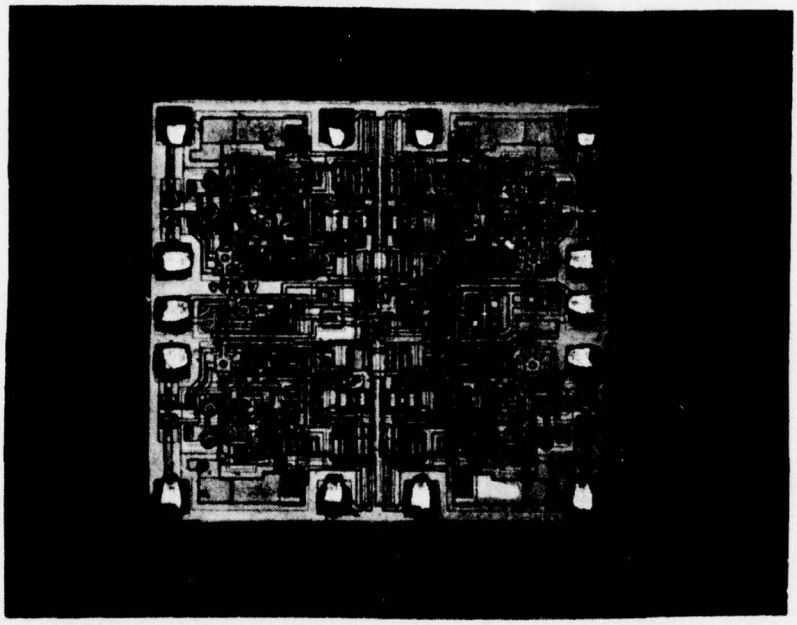

Fig. V-39 Acceptable bond test.

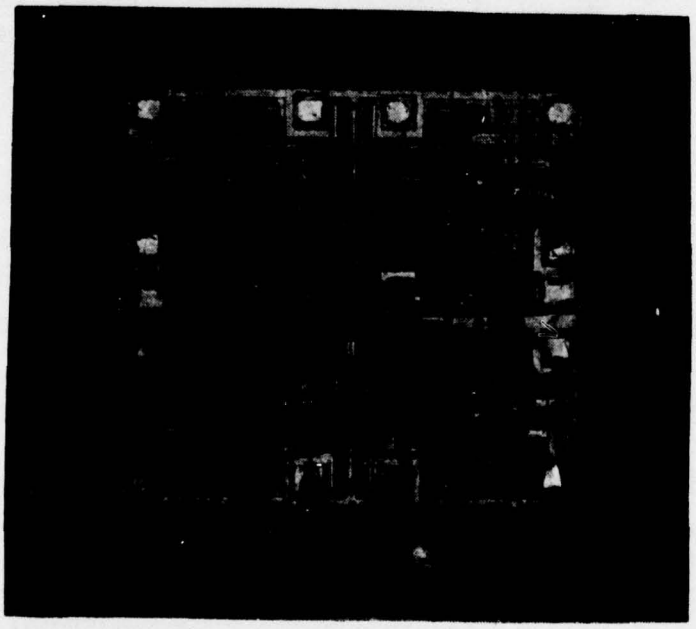

Fig. V-40 Unacceptable bond test.

Fig. V-41 Photomicrograph showing cracking of Si under bump area.

It is believed that the difficulty caused by the Ti-Pd-Au metallization is related to stresses induced as a result of elevated temperature interdiffusion between the Pd and the Au which proceeds at a rate many times higher than that between Pt and Au. As a result of the Pd/Au diffusion, which occurs during the 320°C baking involved in wafer processing, there is considerable lattice disruption, and physical evidence of hardening is visible close to the silicon surface. Two microhardness traverses of a cross sectioned bevel-lapped bond bump are shown in Figs. V-42 and V-43. Reference to Fig. V-43 indicates that the gold bump is of uniform hardness without deviation until the Pt interface is reached. The small indentation indicative of the harder value for Pt is located at the right of the photomicrograph. In distinction, the gold bump hardness increases well away from the Pd location, in Fig. V-42, showing clearly the hardening and strain-induced effect of the diffused region.

It is postulated that since the bump is firmly adhered to the underlying silicon by the intermediate Ti, Si_3N_4, and SiO_2 layers, the rapid thermal shock administered during the inner-lead thermocompression bonding is transmitted to the silicon through a hard, unyielding intermediate layer (PdAu) and that this causes fracture in the silicon as its tensile strength limits are exceeded.

4. Outer-Lead Bonding

Thermocompression bonding of the outer-lead portions of the beam tapes to lead frames is performed on an automatic machine commercially available from the Jade Corporation. The machine bonds at rates up to 4,000 devices per hour. Bonding is feasible to either spot plated (Au or Ag) areas on steel or to a bare Cu alloy lead frame. Typical bond conditions, which are similar regardless of the lead frame alloy are:

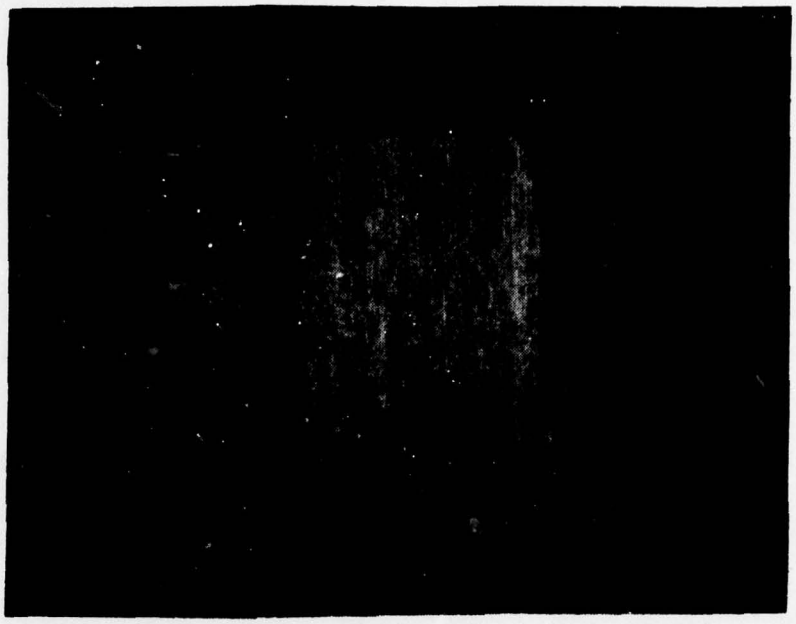

Fig. V-42 Microhardness traverse of a Pd Au bevel-lapped bond bump.

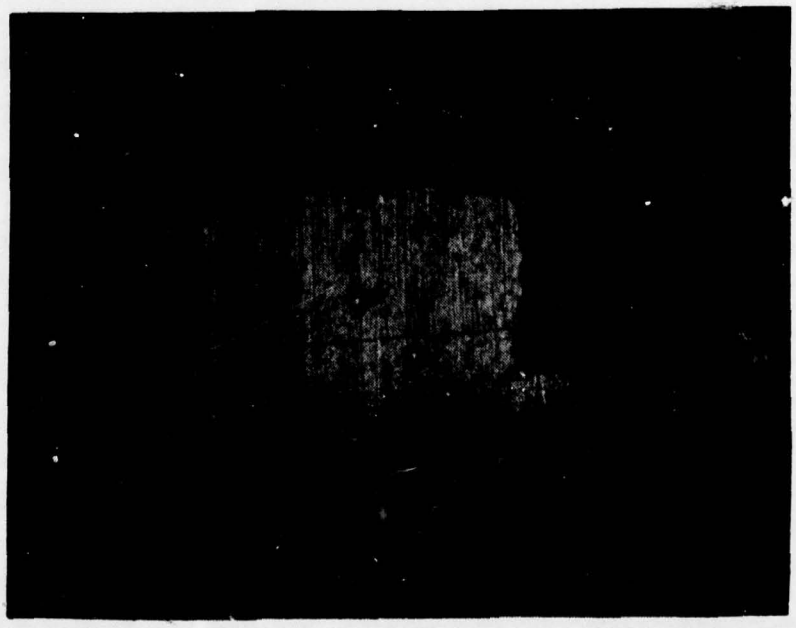

Fig. V-43 Microhardness traverse of a Pt Au bevel-lapped bond bump.

Tool temperature = 600°C
Tool force = 3,000 to 3500 grams
Bond time = 0.5 second

A typical bond to the Cu alloy lead frame, which yields pull strengths of 80 grams to 100 grams, is shown in Fig. V-44 .

Molding Compounds

In order to attain the cost/reliability goals of this program, commercial materials have been used for the dual-in-line plastic packages. The molding compound is a fire-retardant Novolac epoxy formulation used in packaging conventional integrated circuits for normal operation in the range between 125°C and 150°C maximum. This operational range falls well below the 200°C exposure required for accelerated stress testing in order to establish the 0.005%/1,000 hours failure rate set as the principal program goal. As a result of this disparity between established usage and test requirements for the epoxy molding compound, failure mechanisms on the device have been noted at the 200°C test temperature which are not experienced at normal operating temperatures.

This phenomenon is illustrated by the data in Table V-15. These show that epoxy molded devices withstand exposure to ambient temperatures below 175°C without failure. Failures are observed as the temperature rises to 200°C during the 150°C operating life test sequence. These failures are primarily the result of electrical leakage and short circuits. In contrast, no failures have been noted with devices encapsulated with a silicone molding compound.

Examination of failed units has disclosed that the shorts are the result of the redeposition of Cu on the device structural surfaces. The Cu beam tape discloses an etched appearance after

Fig. V-44 Cross section of outer-lead bond to copper-alloy lead frame.

Table V–15 – Elevated Temperature Life Test Data

Device (Test No.)	Molding Compound	Beam Tape Construction	Test Conditions	Hours Exposure	Results Fail/Total	% Fail
CA3046 (1508)	Epoxy	3M, Cu on Polyimide	125°C Operating Life	1000	0/19	0
			150°C Ambient	1000	0/20	0
			175°C Ambient	1000	0/35	0
CA3046 (1600)	Epoxy	3M, Cu on Polyimide	150°C Operating Life T_j = 200°C	48	14/15	95
CA3046 (1602)	Epoxy	3M, Gold Plated Cu on Polyimide	150°C Operating Life T_j = 200°C	48	12/15	85
CA3046 (1562)	Epoxy	Bare Cu No Polyimide	150°C Operating Life T_j = 200°C	168	18/20	90
CA3046 (1604)	Silicone	3M, Cu on Polyimide	150°C Operating Life T_j = 200°C	600	0/10	0

failure such as that which results from a corrosive attack; it is apparent that a chemical reaction has taken place between the Cu and elements of the epoxy molding compound at device temperatures greater than 175°C.

The epoxy compounds used for semiconductor encapsulation are extremely complex combinations of resin, hardener, accelerator, filler, release agents and specific fire retardant additives. The compounds have been formulated to obtain optimal characteristics with respect to thermal expansion, glass-transition temperature, residual chemical impurity content, moisture absorption and transmission, and a host of other parameters that permit large-scale fabrication of molded DIP's. The development of these properties has been directed toward devices that operate in the 125°C and 150°C range; there is only minimal information available concerning operation at temperatures in excess of 200°C.

The corrosive attack on Cu at these temperatures results from a chemical change in the molding compound, which provides a source for this attack. The precise nature of this source has not as yet been clearly defined, but it is postulated that Cl_2, Br_2, NH_3, Sb and other molding compound constituents are liberated to attack and dissolve Cu, and subsequently to permit its redeposition, which leads to degradation of the device metallization.

E. Relative-Cost Comparison

Table V-16 presents relative-cost data for the domestic production of plastic- and ceramic-packaged integrated circuits. The costs are related to yields and cover material and labor. The CA741 14-lead device was chosen to provide the baseline data for the comparison; costs for production levels of 15×10^6 units per year were utilized. In the System I

Table V–16 – Relative Cost Comparison

System Number		I		II	III
System Processes	Passivation	SiO_2		SiO_2	Si_3N_4
	Metallization	Aluminum		Aluminum	Trimetal
	Dielectric Overcoat	CVD PSG		CVD PSG	Si_3N_4
	Device Bonding	Wire		Wire	Beam Tape
	Assembly	Manual		Manual	Automated
	Packaging	Hermetic Ceramic		Plastic	Plastic
Relative Cost Factors	Wafer Process Through Passivation	15		15	15
	Metallization	2		2	6
	Dielectric Overcoat	2		2	2
	Separation	11		11	5
	Assembly	White 250	Frit Seal 65	48	22
	Encapsulation and Test	38	30	22	22
	Total Relative Cost	318	125	100	72

tabulation, both a lidded-alumina, white-ceramic and a two-piece ceramic, frit-sealed package are described. Analysis of this tabulation establishes the following salient points:

- Wafer processing costs are identical through the diffusion and passivation levels.
- Metallization costs for trimetal circuitry and gold bumps are three times those for conventional aluminum metallization, but represent a small part of the total cost.
- Dielectric overcoating costs, whether CVD PSG or plasma-reactor-deposited Si_3N_4, are identical.
- Conventional wafer separation by scribing and breaking introduces yield losses not experienced in the mounted-wafer sawing procedures used for automated assembly and, therefore, yield losses after scribing and breaking are approximately twice those after sawing.
- Assembly costs include those for the package materials. The high costs for the white-ceramic dominate this area, but are diminished for the frit-sealed unit. Manual wire bonding is considerably more costly than automated assembly, and this is the principal factor in the cost differential between the System II and System III data.
- Both hermetic packages require sealing and inspection not applicable to plastic-encapsulated packages; these additional steps are reflected in the higher cost for System I encapsulation and test.
- The cost data for System II were factored to total 100. The data for the others were then compared to these and tabulated in descending order.
- Costs for reliability validation are omitted.

Analysis shows that the lowest production costs are those associated with the automated-assembly System III, and that its cost ratio to that of System II is 0.72. Since these data are for a relatively low-cost device, further information is presented in Table V-17 and V-18 for more costly devices.

Table V–17 – Comparison of Yield-Related Device Costs – 14 Lead						
Cost Factors	Basic CA741 Device Cost		Double Device Cost		Quadruple CA741 Device Cost	
	System II	System III	System II	System III	System II	System III
Wafer Process	15	15	30	30	60	60
Metallization + Overcoat + Separation	15	13	15	13	15	13
Assembly + Encapsulation	70	44	70	44	70	44
Total	100	72	115	87	145	117
Ratio	0.72		0.76		0.81	

Table V–18 – Comparison of Assembly-Related Device Costs – 28 Lead						
Cost Factors	Basic Device Cost		Double Device Cost		Quadruple Device Cost	
	System II	System III	System II	System III	System II	System III
Wafer Process	15	15	30	30	60	60
Metallization + Overcoat + Separation + Encapsulation	37	35	37	35	37	35
Assembly	96	22	96	22	96	22
Total	148	72	163	87	193	117
Ratio	0.49		0.53		0.60	

The basic assumption for the devices used for review in Table V-17 is that the devices are intended for 14-lead packages, and that the increased cost is related to such yield factors as chip size, circuit complexity, and electrical requirements. The data indicate that, as the cost of the chip increases, the cost advantages accruing to automated assembly decrease in comparison to those for manual wire bonding.

An additional vital factor to be considered in evaluating device costs is that related to assembly. Table V-18 presents data for the basic, double, and quadruple yield-related device costs as they are affected by an increased number of bonding sites. For a 28-lead DIP, the manual wire-bond assembly costs will be doubled compared to those for the 14-lead DIP considered above. However, since all bonds are made simultaneously in automated assembly, there are no additional costs for this procedure.

Analysis of Table V-19 which summarizes data from both of the preceding tables, shows that:

- Automated assembly of a basic, 14-lead, low-cost device offers a cost advantage ratio of 0.72.
- Automated assembly of yield-related costlier devices diminishes this cost advantage.
- Automated assembly of assembly-related costlier devices enhances this cost advantage.

Table V–19 – Cost Data Summary

Number of Leads	Basic Device		Double Cost Device		Quadruple Cost Device	
	System II	System III	System II	System III	System II	System III
14	100	72	115	87	145	117
28	148	72	163	87	193	117

System III/System II Ratio Summary			
Number of Leads	Basic Device	Double Cost Device	Quadruple Cost Device
14	0.72	0.76	0.81
28	0.49	0.53	0.60

SECTION VI

RCA PROPOSALS TO GOVERNMENT AGENCIES UTILIZING CONTRACT-RELATED TECHNOLOGY

DSG 77-688-004, DAAG 39-76-R-9396, 19 January 1977 Development and Production of XM734 Amplifiers and Custom Integrated Circuits. Submitted to Harry Diamond Laboratories, 2800 Powder Mill Road, Adelphi, MD 20783.

DSG-77-588-006, DAAB 07-77-Q-0355, 20 January 1977 Manufacturing Methods and Technology (MM&T) Program for Automatic Separation, Carrier Mounting and Testing of Semiconductor Dice.
Prepared for Communications Systems Procurement Branch, Procurement and Production Directorate, U.S. Army Electronics Command, Fort Monmouth, N.J. 07703.

SECTION VII
PHASE II PROGRAM

Phase II, the low-cost high-reliability device-fabrication phase of the program, will involve significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits will be constructed in both plastic and ceramic packages. This plan will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes will be defined and documented. The utilization of existing equipment and mask sets will be demonstrated, and the cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions at wafer probe and final test will be used to monitor the production run and to assure process reproducibility. Devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and assembled. The milestone chart for Phase II is shown in Fig. VII-1.

As shown in Fig. VII-2, the minimum quantity of units required for delivery to the Navy and for the Phase III test plan is 5165 devices per type. Reliability testing during Phase II will require additional units, and other needs will surface during the course of the contract. It is anticipated, therefore, that approximately 10,000 units of each device type will be fabricated during Phase II.

In addition to initiating the long-term 125°C life tests during Phase II, a program of accelerated life testing is planned for two circuits,

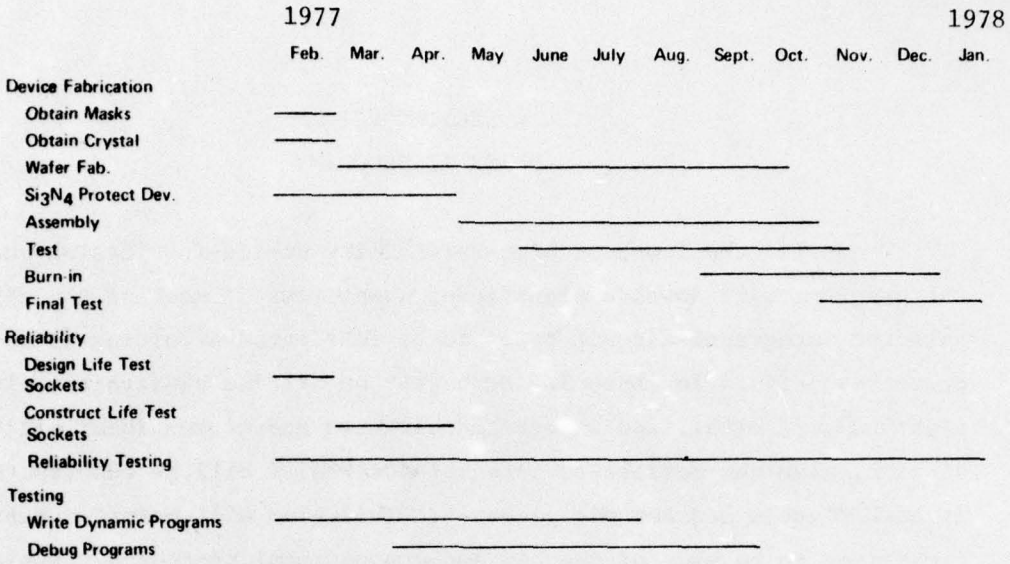

Fig. VII–1 – Phase II Milestone Chart.

Type	CD4012B	CD4014A	CD4027B	CA741	5420	54S20	5470	5472
Technology	COS/MOS	COS/MOS	COS/MOS	Bipolar Linear	Au-T^2L	Schottky	Au-T^2L	Au-T^2L
Wafer Lot Size	25	25	25	25	25	25	25	25
Net Units Required								
Internal								
Al DIP	115 →							
Al DIC	145 →							
Trimetal DIC	155 →							
Trimetal DIC (Unencapsul.)	25 →							
Trimetal DIP	725 →							
To Be Delivered	4000 →							
Total	5165 →							

Fig. VII–2 – Phase II Device Fabrication Plan.

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the CA741 and the CD4012B. This program will verify that the reliability goals of the program are being met, compare the encapsulation techniques, and compare the results achieved with devices in dual-in-line ceramic packages. The planned test matrices are shown in Fig. VII-3.

Life Tests	Encapsulation Technique				
	Silicone	Epoxy Novalac	Epoxy Novalac With Junction Coat	DIC	Non-Hermetic DIC
Bias					
150°C	20	20	20	15	15
175°C	20	20	20	15	15
200°C	20	20	20	15	15
225°C	20	20	20	15	15
250°C	20	20	20	15	15
Storage					
150°C	15	15	15	10	10
175°C	15	15	15	10	10
200°C	15	15	15	10	10
225°C	15	15	15	10	10
250°C	15	15	15	10	10
Step Stress					
150°C	20	20	20	15	15

Types: CD4012B, CA741

Fig. VII-3 Phase II test plan.

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